Towards a New Approach to Concurrent Thermal Design of PCBs

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Abstract

A thermal design methodology suitable for concurrent design of cost-driven electronic systems is proposed and exemplified for a sample printed circuit board (PCB). The design methodology utilizes an evolutionary concept, in which the analysis tools are capable of adjusting their level of complexity as the design evolves, initiating with rough approximate analyses and culminating with a conjugate conduction/convection simulation for a portion of the sample of the PCB. The level of approximation included at each stage is selected with consideration of both time and accuracy constraints. The importance of considering the conjugate problem in generating heat transfer coefficients for electronic packages is discussed. The proposed thermal design methodology is then applied to the Vu-Man artifact and the results are described to illustrate the effect that upstream thermal information can have on the evolution of a design.

Nomenclature

c_p = specific heat
h = heat transfer coefficient
h_{ave} = row-wise average heat transfer coefficient
H = half channel height
L_{row} = length of row
q" = heat flux
Re = Reynolds number = U_{max} H ρ/μ
T_∞ = ambient temperature
T_{chip} = temperature of the chip
$T_{mixed\text{-}mean}$ = mixed-mean temperature
$T_{mixed\text{-}mean\ row}$ = row-wise mixed-mean temperature
U_{max} = maximum velocity

Greek Symbols

ρ = density
μ = dynamic viscosity

Introduction

The advances achieved in the design and manufacturing of integrated circuits have resulted in a dramatic improvement in performance and reduction in size. However, this reduction in chip size has increased the heat flux of each chip. Chip heat flux is rapidly approaching, and in some cases, exceeding values commensurate with a nuclear detonation, yet many chips have recommended operating temperatures in the 90°C range [1]. Additionally, gallium-arsenide field effect transistors, one of the many possible arrangements suggested for future use, have a permissible operating temperature in the 0°C range [1]. Therefore, resultant heat fluxes will need to be dissipated with only minimal increases in temperature. Coupled with these increasingly challenging technical problems are the pressures from the highly competitive marketplace. These pressures are forcing designers to synthesize products in a competitive time frame that have vastly superior performance and are also inexpensive to produce and maintain. In addition, adjustments to satisfy specific design domain constraints often pose downstream problems in other domains, which may lead to design iterations, delay, and cost increases.

These factors have fostered interest in the concept of concurrent design, through which the contributions of various required, but isolated disciplines may work in parallel. It is hoped, through the successful application of concurrent design methodology, that downstream concerns may be brought forward in the design cycle with the objective of reducing thermally-caused failures and shortening the design cycle and time-to-market.

A complementary approach to concurrent design involves the formulation of a design methodology, which when coupled with the proper tools, provides feedback in the form of suggestions to the designer. This would permit a relatively inexperienced thermal designer to create designs accounting for a variety of plausible alternatives. Therefore, the proposed thermal design methodology is formulated with the intent of allowing exploration and evaluation of design alternatives. The successful application of such a thermal design "advisor" strategy would insure that a wide spectrum of options are considered in order to select the best suited to cool the electronic system.

Motivation

In the past, cooling an electronic system was merely an afterthought. A fan was added to the system and expected to properly cool all the constituent components. Unfortunately, not all the components received enough air flow and some of the resultant systems have proven to be unreliable. Today, as limitations in product development arise from the inability to achieve adequate cooling, the importance of thermal design is self-evident. Furthermore, although Level I technology (I.C.'s and chips) has been successfully miniaturized, improper thermal design may not necessarily permit size reduction of the total system [2]. Therefore, thermal management concerns need to be addressed early in the design cycle to achieve adequate cooling in the most advantageous manner.

Once an initial informational overhead has been overcome, mechanical, electrical, esthetic, and other important factors may be accounted for and integrated into the design. In this fashion, it is hoped that problems may be circumvented before the production of a prototype. However, many hindrances can cause this design philosophy to be exceptionally difficult to implement. Lack of communication, contrasting design goals and philosophies, differing technical jargon, and unclear establishment of priorities can make concurrent design extremely difficult to implement and ineffective in improving overall results [3]. Therefore, individual design methodologies may require alteration to accommodate a concurrent design framework.

In a concurrent design framework, parameters are dynamic and the value of information is related to its timeliness as much as to its accuracy. This may be troubling to a designer who has frequently worked in isolation, because the designer was able to apply the most powerful tools available and produce data of the highest confidence. However, in the concurrent design setting, parameters are changing as other factors are taken into account. This is exemplified in the thermal management area through the design of an air-cooled computer cabinet or housing. The cabinet

serves a multitude of purposes, although many may seem unrelated.

The cabinet has to be esthetically acceptable while satisfying structural and accessibility constraints. However, modification in the shape of the cabinet to accommodate any of the above factors may have a significant impact upon the system's thermal performance. This is because convective performance is directly related to the flow paths of the cooling fluid. Therefore, before any final thermal analysis is conducted, the housing must be fully specified. However, it is impossible to complete the design of the housing without specifying if a fan or similar forcing device must be accommodated, as well as the desired orientation and placement of the constituent boards and other components. Therefore, many or all of these factors require simultaneous consideration to achieve the optimum, or near optimum, cabinet design.

In cost-driven systems, alternatives must be carefully evaluated and implemented keeping in mind the philosophy of diminishing return. For example, it may be possible for the electrical engineer to select a different chip carrier and in so doing, allow for natural convection cooling as opposed to forced convection. As the variety of chip carriers increases, it will become more difficult to select the most thermally and economically appropriate carrier. Replacing plastic chip carriers with ceramic carriers may not be necessary for all the components in a system. Selective use of advanced chip carriers will result in the most economical solution. Such alternatives must be determined early if they will have a chance of being advantageously integrated into the final design. Additionally, taking into account thermal constraints before the electrical design has been finalized may lead to systems far more reliable and less expensive to use and maintain. However, in the early stages of design, it is often time prohibitive to perform highly-accurate thermal analyses of a system. Therefore, the objective of this paper is to propose and implement a concurrent thermal design methodology that increases in complexity and refinement as the design cycle matures. This thermal design methodology must be independent of physical prototypes and capable of both conducting analyses and proposing alternatives.

Independence from physical prototypes usually necessitates a numerical or analytical approach. In general, the complexity of electronic systems strictly limits the usefulness of analytical approaches. Therefore, numerical approaches are often utilized and can be classified as either conduction-only or conjugate conduction/convection methodologies.

The conduction-only simulation requires the specification of heat transfer coefficients for environmentally exposed surfaces. Subsequently, the heat equation is numerically solved either with a thermal network or finite element technique. Thermal networks, in which the physical system is approximated by a series of equivalent thermal resistances, have been proposed and successfully implemented by many researchers [4-6]. However, in many cases, such a lumped formulation is inappropriate and may yield erroneous results. Proper judgment as to the number and placement of thermal resistors is extremely essential for accurate results [7]. Alternatively, the finite element method has been successfully applied to individual components [8-10]. This approach accounts for more than one-dimensional heat flow paths, but is much more time consuming than a thermal network.

The conjugate conduction/convection approach involves the simulation of the conduction within, and the convection from, the components. This is done through the solution of both the Navier-Stokes and energy equations for the fluid, and the heat equation for the solid. The benefit of this approach is its independence from assumed heat transfer coefficients. The major drawback is that the simulation is extremely time consuming, especially when the Navier-Stokes and energy equations are non-linearly coupled, as would be the case if buoyancy effects are taken into account.

The conjugate solution of uniformly heat generating components on air-cooled electronic boards, in two-dimensional flow configurations, is reported in [11-13] using the Simpler algorithm [14]. All of these flows were assumed to be time independent, which limits their applicability to only steady flows. However, researchers have determined that flows in electronic board configurations are time dependent for certain Reynolds number ranges [15-17].

The results obtained from the conjugate solutions are the most complete and accurate simulations of the modeled problem. However, because of time constraints, it would be inappropriate to use the complete conjugate simulations in all but the final stages of a concurrent thermal design. Therefore, an approach will be outlined in the next section that will initiate with

very rough analytical calculations, progress to the conduction simulation, and culminate in the full conjugate conduction/convection analysis.

Thermal Design Methodology

A five-stage approach is presented, which allows the thermal designer to fully participate in a concurrent design environment. Each stage is formulated to address specific issues that would require resolution to enable other design disciplines to contribute, accounting for thermal considerations. As the concurrent design evolves, preliminary solutions are analyzed and corrections are suggested until a design is produced that satisfies the specified constraints.

The concurrent thermal design framework is envisioned to be independent of previous thermal design experience. Such experience would allow a designer to skip some of the initial calculations that will be outlined in the earliest stage of the design. However, whether these issues are resolved from previous experience or with the use of primitive calculations, they would still require resolution before proceeding to the next stage. Additionally, this design approach is dependent upon a numerical analysis package that is capable of solving the heat equation, Navier-Stokes equations, and the conjugate conduction/convection problem. While many numerical approaches satisfy these requirements, the Spectral Element method was selected. This method combines the competitive advantages of both the finite element and global spectral methods. It therefore permits natural treatment of complex geometries, such as those encountered in electronic systems, while providing spectral accuracy. The achieved level of accuracy and computational efficiency allows for the direct simulation of flows in laminar and transitional regimes. Furthermore, with the use of static condensation and high order interpolants, the Spectral Element method permits advantageous implementation on parallel computer architectures.

Stage One

The Stage One thermal analysis is conducted after the electrical design has been completed to the point of specification of all chips, their associated carriers, and relative positions upon a Printed Circuit Board (PCB). However, these would only be initial specifications, for the requirements of other designers may mandate alterations. It now becomes necessary for the thermal designer to address several basic, but very essential issues: *Can the initially specified electrical design be adequately cooled? If so, through which cooling arrangements?* The resolution of these issues can be achieved by approximate analyses.

Once the packages are specified, the power generation, dimensional and material data, and acceptable operating temperatures are available. Then, it is possible to approximately determine the average heat transfer coefficient required for adequate cooling (eq. 1). Diagrams that display the relative thermal performance of different cooling methods [18,19] are also useful for this purpose. The thermal designer would convey all the possible alternatives to the entire design group for discussion.

$$h = \frac{q''}{(T_{chip} - T_{mixed\text{-}mean})} \qquad (1)$$

This initial discussion enables evaluation of different cooling arrangements with respect to many constraints. For example, if the system is to be strongly constrained acoustically, then a natural convection solution would be appropriate. Therefore, strict limits upon power output or total board area would have to be addressed. Alternatively, replacement of the initially specified chip carriers or the addition of fins, heat sinks, or heat pipes might be required. All of these alternatives have to be considered and weighed against other goals of the design. Once this stage has been completed, the basic type of cooling configuration will be specified. The other designers would continue with their analyses, accounting for the ramifications of the selected cooling arrangement.

It would be inappropriate at this stage to resort to very detailed analyses, because only rough estimates are required to allow for meaningful participation. Also, other designers would be unable to participate until these high-level specifications are determined. An experienced thermal

designer would probably be capable of addressing many of these issues without conducting any calculations.

Stage Two

After a cooling alternative is specified, thus allowing other designers to account for its associated ramifications, the Stage Two thermal analysis is conducted. The basic goal of this stage is to *confirm the effectiveness of the thermal design specified in the previous stage*. This is done through a conduction simulation, using an assumed average value for the convective heat transfer coefficient, as explained below. This permits a rapid assessment of the Stage One cooling configuration and provides local thermal information that indicates the probability of chip carrier replacement. However, the results at this stage are highly dependent upon the value of the specified heat transfer coefficient.

Much experimental research has been conducted in an attempt to establish empirical heat transfer correlations for electronic equipment and systems. These resulting correlations have ranges of applicability, both in terms of geometry and Reynolds number. Therefore, a designer must select the correlation that was developed for the most similar case to the actual system being analyzed. Most of the work was conducted for periodic domains, in which the electronic packages were identical. This situation is fairly uncommon in actual electronic systems. Furthermore, missing packages can have a substantial effect upon the overall thermal performance [20]. A thermal analyst must therefore select the most applicable correlation from those available [21]. The Reynolds number would then be selected to yield a value commensurate with the cooling requirement indicated in the Stage One analysis. Once this specification has been made, the steady heat equation can be solved yielding a temperature distribution for the system and its constituent components.

It must be stated that to include any more details at this stage would be wasteful and inappropriate because very little of the physical design will have been specified. The housing designer has not yet placed many of the largest components within the cabinet, such as the power supply, disk drive(s), and supporting structures. Furthermore, the general orientation of the board(s) within the cabinet may not have been specified. Therefore, it would be fruitless to involve any more complexity in the analysis, such as entrance and exit effects, or other large-scale flow phenomena, because far too many permutations would require simulation. However, the results of this purposely approximate simulation are quite useful. Other than a general verification of the specified cooling arrangement, local temperature distributions are determined for each component. This information gives the designer an indication as to the possible existence and location of thermally problematic regions.

Alternatively, the areas of the board producing the highest temperature rise are determined, thereby permitting thermal considerations to be included in the specification of board orientation and placement of other heat producing components. Additionally, because of the direct relationship between temperature and Mean Time Before Failure (MTBF), accessibility considerations can account for locations of components with the lowest predicted MTBF. Although final specification of chip carriers and board orientation would still require determination, basic characteristics of the system's thermal performance may be taken into account. Additionally, a preliminary cost could be estimated for the initial specification of chip carriers. This yields an early indication as to whether the initial thermal design permits a within-budget, final product. The other major advantage of the generality of this analysis is the relative ease with which many alternatives may be considered. This allows for alterations in the initial specification without requiring an entirely new thermal analysis.

Stage Three

This stage initiates after specification of board orientation and placement of the power supply and disk drive(s). The previously assumed, average heat transfer coefficient for the entire board and constituent components is substituted with an average coefficient for each component. A modular approach is used, which requires general categorization of the basic flow regime, as well

as geometrical and Reynolds number specification. In this manner, *large scale flow phenomena are accounted for in the model.* The modular approach combines the previously generated correlations and associated perceived flow patterns, enabling amalgamation of these data in a design useful format This allows the designer to have a preliminary indication of die overall thermal performance ef the system, accounting for large-scale flow effects.

First, each board is subdivided into different regions based upon whether the thermal and fluid fields are fully developed. Each region is treated separately, thus enabling variability in the mixed-mean temperature and heat transfer coefficient correlation for each successive component. The variation in thermal performance for each successive row will asymptotically approach the periodic fully-developed condition. Therefore, an exponential-like curve represents die convective performance for each board. In the upstream region, special correlations account for entrance effects [12], whereas in the fully-developed region, the value of the heat transfer coefficient remains approximately uniform. However, if the components are not geometrically similar, as often is the case, different correlations are used for each component. Although this approach inevitably results in approximate calculations, the nonlinearity in thermal performance provides very few alternatives. Additionally, this type of analysis has a built-in safety margin, because the geometrical non-homogeneities usually induce better mixing and therefore more effective cooling flow patterns.

The results of this stage's analysis enable a more precise estimation of the MTBF and a further verification of the adequacy of the cooling configuration. As in the previous stage, many different alternatives may be explored with relatively little modification. Additionally, no alteration of the Stage Two discretization of the computational domain is required. Moreover, if increased numerical resolution and accuracy is desired, this is achieved in the Spectral Element method, like in p-type finite element approaches, by increasing the oider of the local interpolants.

Stage Four

The goal of this stage is to *obtain the best possible results for the conduction-only simulation.* The effect of local vortical structures and other small-scale flow patterns will be accounted for in the specified heat transfer coefficients. This requires designation of the local flow pattern existing between electronic components (groove), as one of the following: (a) only one large vortex, (b) a complex pattern of vortex growth and absorption, and (c) direct impingement by the bypass flow into the groove [21]. Additional specification will be required, consisting of a basic geometric description of the groove and relative dimensions of its sides. With this information, it becomes possible to include a spatial corrector [22], which varies the magnitude of die component-averaged, heat transfer coefficient along die surface of each package. An alternate approach has been proposed [23] that accounts for the growth of the thermal and fluid boundary layers along components by approximating the packages as flat surfaces. In doing so, it becomes possible to apply analytic boundary-layer solutions to estimate local heat transfer performance. However, this approach neglects flow phenomena, such as separation and recirculation, usually associated with component geometries.

The resulting simulations provide the maximum level of confidence for the temperature fields obtained with the conduction-only approach. Consequently, calculations for the MTBF can be conducted for all the components, enabling final indication regarding overall reliability. In addition, stress concentrations for the board can be determined from the resulting temperature fields, providing the necessary information to modify the support structure to minimize stress concentrations. Individual package temperature distributions are obtained, enabling a final decision as to the replacement of any chip carriers. This permits an equivalency in component reliability, which would finalize the overall chip carrier selection process. Furthermore, regions that might be candidates for turbulators or flow mixers can be identified. For example, the insertion of turbulators in the flow field may be desirable rather than having to increase the Reynolds number of the flow or replacing many of the packages with more expensive chip carriers. The decision to make any of these modifications may have a global effect upon the overall design and its associated cost. Therefore, the detailed level of information that this analysis would supply permits educated

selection of enhancement alternatives.

Stage Five

This stage consists of the final prototype-independent thermal analysis. The housing design is fully specified, as are all die other physical parameters of the design. It would be the goal of this stage ***to provide the mast accurate information regarding the thermal design.***

A conjugate conduction/convection analysis is carried out for either specific regions or the entire system. This stage is the last chance for the thermal designer to correct any thermal problems before the construction of the prototype. Any thermally-problematic regions identified after the construction of die prototype may necessitate an additional design iteration. Reduction or elimination of additional design cycles is die goal of concurrent design.

In keeping with this philosophy, each designer conducts the most accurate analyses of which they are capable, to insure the adequacy of their aspects of the total design. Since all of the design parameters are static at this level of design maturity, the disciplines are working individually. It is for this reason that the time required to conduct an accurate conjugate conduction/convection simulation is acceptable. Unfortunately, even with the rapid advancement in computational capability and memory, most electronic systems are too large and complex for a complete treatment Initially, it may be desirable to examine only a section in the folly-developed region, since the highest mixed-mean temperature exists in this region and therefore the poorest thermal performance. In the near future, as the speed and memory of computers increase, so would the size of the sub-domain to be simulated. However, even the results corresponding to a sub-domain are extremely useful in order to correct, improve, and/or construct geometric correctors and empirical heat transfer correlations. Additionally, the results provide an indication as to the overall accuracy of the Stage Four analysis. If a design is found to be acceptable after die Stage Five analysis, the thermal designer approves the construction of the prototype. The testing of the prototype is the final check of the thermal design, but its associated procedures are beyond the scope of the envisioned thermal design framework.

Example Implementation

In this section, the concurrent thermal design framework outlined above is demonstrated upon a sample board. It is presented as a thermal design iteration, which allows for other design disciplines to participate periodically throughout the design evolution. However, to folly judge its relative merit as a thermal design procedure, data from many actual concurrent implementations are required.

The board to be cooled consists of twelve rows of uniform, surface-mounted components, each producing 0.3 watts (Fig. 1). The composition and internal structure of the components, depicted in Fig. 2, is chosen to include all relevant parts of a typical package, allowing the application and description of the various stages of the concurrent design methodology.

Stage One

As previously described, die purpose of this stage is to determine the possible means by which adequate cooling can be achieved for the sample board. The first step will therefore involve determination of the surface heat flux and specification of the average surface temperature along the component For the sample board, the uniform surface heat flux per unit depth corresponds to 7.16×10^{-2} watts/cm for the prescribed package and chip size. Additionally, the ambient and inlet temperature is specified as 25°C and the desired average surface temperature for each package is 80*C, yielding a temperature difference of 65°C. This information, with the aid of Fig. 3a, indicates that air cooling is a possible alternative. However, as the flow of air passes over successive rows of components, its temperature increases, resulting in smaller permissible temperature differences.

This is an important consideration because although the average conditions may be favorable for air cooling, the final rows of packages may not satisfy die specified operating conditions. An energy balance is applied to model the rise in mixed-mean temperature of the cooling fluid. The

resulting expression (eq. 2) indicates that for the specified heat flux, the mixed-mean temperature will rise 2.23°C per row at Re=648. This Reynolds number is determined iteratively, where the calculated ΔT (eq. 2) must yield the highest heat transfer coefficient obtained from the lumped analysis and also achieve the same heat transfer coefficient with the correlation used for the Stage Two analysis. Therefore, rather than a single operating point, a row-wise operating range exists as indicated in Fig. 3b.

$$\Delta T_{mixed\text{-}mean_{row}} = \frac{3\, q''\, L_{row}}{4\, \mu\, Re\, c_p} \qquad (2)$$

Although the initial rows might be adequately cooled through natural convection, the final rows require forced convection cooling. Table I indicates the required average heat transfer coefficient per row, calculated with respect to an average surface temperature of 80°C. It should be noted that although the average surface temperature is 80°C, the chip temperature would be higher. This is the drawback of a lumped-analysis approach. Therefore, the specified average surface temperature must be carefully selected accounting for component geometry and material properties.

The thermal designer reports this information to the design group and a decision is made as to whether the preliminary thermal design, forced-convection air cooling is acceptable. The proposed thermal design requires that the housing designer accommodates a fan and an outlet and inlet for the coolant flow. Additionally, the exiting air temperature, predicted to be about 50°C, would need to be diverted away from the user.

Row	$T_{mixed\text{-}mean}$ (°C)	h_{ave} (W/m^2 °C)
1	26.11	13.29
2	28.34	13.87
3	30.57	14.49
4	32.80	15.17
5	35.02	15.93
6	37.24	16.75
7	39.47	17.67
8	41.70	18.70
9	43.92	19.86
10	46.15	21.16
11	48.38	22.65
12	50.60	24.37

Table 1

If any of the consequences predicted by the preliminary thermal analysis are unacceptable to the design group, then the initial electrical design requires alteration. Alternatively, other cooling configurations could be considered, for example liquid cooling, including natural convection, forced convection, and boiling, or perhaps the use of heat pipes. However, the group's response is specified as accepting the forced-air, direct-cooling strategy. Regardless, an important benefit of a concurrent design strategy is already obvious, that is the *awareness of the entire group to the consequences of the thermal management strategy as well as their participation in the selection process.*

Stage Two

The next stage in the thermal design involves the conduction-only simulation for the board. Firstly, a discretization must be specified which accounts for both the required time for entry, as well as the computational time, memory requirements, and accuracy. The computational domain is

subdivided into three separate meshes, each consisting of about two-hundred elements (Fig. 4). The advantage of the domain division is that only one-third of the domain needs to be discretized and that a satisfactory number of elements may be placed within each component. The drawback is that conduction through the board is limited to only three sections, requiring modeling of conduction through the ends of the board. However, the savings in both entry and computational time outweigh this disadvantage.

The convective heat transfer coefficient must be determined by selecting the most appropriate correlation available. The correlation presented by Lehmann and Wirtz [24] was selected although it does not exactly satisfy the current board configuration in the distribution of the uniform flux boundary condition along the surface of the package and the geometrical/dimensional range. However, the resulting value for Re=648, or Re=1296 by their definition, agrees well with previous simulations conducted by the present authors for similar geometries. This value of the heat transfer coefficient will be specified for all the forced-convective surfaces. The top surface of the upper board is specified as being adiabatic and the bottom surface of the lower board is specified as having a natural convective boundary condition with $h=0.5\ W/m^2{}^\circ C$ (Fig. 5).

The material properties of the solid region are specified in accordance with Table II. However, effective conductivities are used to account for the lack of intimate contact between surfaces. These values are based upon those suggested by Kraus and Bar-Cohen [18]. The inclusion of the contact resistance is essential to simulate the actual conductive performance of the various components [25]. Additionally, within each element, a seventh-order Chebyshev polynomial is prescribed for each direction, yielding forty-nine degrees of freedom per element.

Material	Thermal Conductivity (W/m °C)
Beryllia	218.0
Silicon	147.0
Thermal Grease	0.669
Aluminum	216.0
Copper Alloy	264.0
Fiber Composite	1.7
Plastic	0.260
Solder	63.0

Table II

The results depicted in Figs. 6a-c support the initial assertion of the Stage One analysis. First, the forced-convective, air-cooling strategy has resulted in adequate cooling with all of the chip temperatures below 80°C. In fact, the average component surface temperatures are all below 80°C. This is because heat is removed from the bottom of the board through the imposed natural convective boundary condition. This was not accounted for in the Stage One analysis.

Due to the symmetry of the board, components, and heat generation, no preference in terms of orientation is substantiated. However, the latter components will operate under the most thermally adverse conditions and therefore, maintenance openings should be positioned to provide preferential accessibility to the latter half of the board. This information is provided to the housing designer. The housing designer could begin to place some of the larger components accounting for the board's thermal characteristics.

Stage Three

The orientation of the board has been specified and therefore, entrance effects are accounted for through the implementation of a particular correlation for the initial rows. The correlation selected is from Davalath and Bayazitoglu [12], and differs from the current geometrical situation in the number and geometric dimensions of the packages. Nevertheless, the correlation is implemented

yielding an exponential decrease in heat transfer coefficient values from the first to the third row (Fig. 7a). It is interesting to note that for the geometry analyzed by Lehmann and Wirtz [24], fully-developed conditions existed after the third row.

The results, depicted in Figs. 8a-c, demonstrate a decrease in the temperature of the first row, with a diminishing effect as the value of the heat transfer coefficient decreases. However, the resulting lower temperatures in the front portion of the board would help to cool the entire board through conductive effects, something that the selected discretization cannot depict.

Stage Four

The specified values for the heat transfer coefficient for this stage account for local flow effects. By classifying the groove between the packages as symmetric with dimensional ratios yielding vortex interaction with the main flow at this Re, it is possible to implement a spatial corrector as indicated in [22]. The spatial corrector is based upon an identical geometry with a uniform flux boundary condition along the board and component surfaces. This results in a spatially-varying heat transfer coefficient for each row (Fig.7). The fully-developed heat transfer coefficient ranges from approximately 8 $W/m^{2*}C$ at the upstream corner formed by the board and component to 35 $W/m^{2*}C$ at the leading edge of the top surface of the component.

The resulting calculated temperature fields differ in row-wise temperature range, as well as the distribution of temperature within the packages (Figs. 9a-c). These temperature fields can be used to simulate the asymmetric, thermally-induced stresses within each package. Additionally, the predicted temperatures for the chips can be used to obtain a MTBF for each component. These results are presented to the design group and a decision is made as to whether an acceptable level of reliability has been achieved with the direct-air, forced convective cooling strategy at this flow regime. Should an unacceptable level of reliability be determined for any of the components in the system, local corrective measures would be implemented, such as replacement of the initially specified chip carrier, inclusion of a fin, or placement of local mixing enhancers.

Stage Five

At this stage, the overall design has progressed to the point where all design parameters are static, so each designer performs the most accurate simulations of which they are capable to insure the adequacy of their aspect of the total design. Therefore, a conjugate conduction/convection simulation is performed by the thermal designer. Unfortunately, computer limitations prohibit a direct numerical thermal-fluid simulation of the entire board. Instead, the simulation is restricted to only one package within the periodic fully-developed region. By doing so, the thermal designer may compare the resulting heat flux and heat transfer coefficient distributions with those corresponding to the Stage Four spatial corrector. This provides an indication as to the accuracy of the operating temperatures predicted in Stage Four.

The instantaneous cooling-fluid flow patterns, illustrated by velocity vectors (Fig. 10a) and contours of the streamfunction (Fig. 10b), indicate waviness in the channel region and the presence of a large vortex in the groove, which is displaced towards the downstream component face. This instantaneous velocity field is a portion of a periodic cycle of vortex growth, absorption, and decay that is common for similar geometries in transitional flow regimes [22]. Such time-periodic oscillating flows have been found to enhance heat transport phenomena.

The corresponding instantaneous temperature field is shown in Fig. 11, in which the temperature ranges from 39.19 to 109.4°C. The vortex at the upstream component face removes heat from the component and convects it back into the groove. Additionally, the vortex serves to convect the thermal wake from the upstream component into the groove. These two effects combine to increase the temperature of the fluid contained in the groove beyond that of the board, resulting in heat transport into, rather than out of, the exposed board surface. This is clearly shown in Fig. 12 where the cycle-averaged heat flux for the exposed board surface (0.00 to 1.25cm and 3.75 to 5.00cm) is negative.

The heat flux distribution along the top surface of the package (Fig. 12) behaves like a developing thermal boundary layer over a flat plate, save in the vicinity of the chip. In this region,

there exists a local rise in the heat flux. This local conjugate effect would be absent from a simulation where the entire component, instead of the chip, is generating heat.

The calculated, cycle-averaged heat transfer coefficient based upon the standard definition (eq. 1) for the conjugate simulation differs from that calculated for the constant-flux boundary condition (Fig. 13). The conjugate, unlike the constant-flux, heat transfer coefficient is negative in some regions because of the negative heat flux.

To determine the effect of implementing the constant-flux heat transfer correlation on the predicted operating temperatures, a conduction-only simulation is conducted based upon the constant-flux heat transfer coefficient and a mixed-mean temperature of 69.76°C. The resulting temperature field, shown in Fig. 14a, demonstrates marked differences from the corresponding temperature field for the conjugate simulation, shown in Fig. 14b. The conduction-only simulation underpredicts the maximum chip temperature by approximately 13°C. If this difference is indicative of the accuracy of the Stage Four simulations, the latter components may operate at temperatures in excess of 80°C. The thermal designer would therefore report to the group the possible requirement of enhancement techniques for the latter rows.

Vu-Man

Stages Four and Five of the proposed thermal design methodology will next be applied to a portable electronic viewing device, called the Vu-Man. The Vu-Man is the culmination of the EDRC-Bosch course conducted during a 14-week period in the summer of 1991. A cross-section of the Vu-Man that includes the electronics and housing is shown in Fig. 15. The electronics of the Vu-Man are mounted on two PCBs. Most of the electronic packages are different, both in terms of geometry and composition, as well as the amounts of heat dissipated. Furthermore, the portable nature of the device mandates strict size and power constraints, necessitating a natural convective cooling configuration.

As previously described, the Stage Four analysis requires the specification of the heat transfer coefficients along all of the environmentally exposed surfaces. This procedure was applied to the lower board and its constituent components. An increasing value from 0.5 (at the bottom of the board) to 10 W/m^2 °C (along the surfaces of the fin) was specified along the individual package and board surfaces, and the ambient temperature was specified as 25°C. The results depicted in Fig. 16 exhibit a maximum temperature of 131.8°C and a minimum of 30.27°C. Since many packages require operating temperatures in the 90°C range to insure acceptable levels of reliability, the thermal performance of the lower board, as indicated by the Stage Four analysis, would be unacceptable.

The corresponding Stage Five analysis yields both the thermal and fluid fields (Fig. 17a,b). Since both the Navier-Stokes and energy equations are simulated no specification of thermal boundary conditions is required along the board or component surfaces. The resulting maximum temperature is 98.27°C and the minimum is 27.87°C. A disparity of 33.5°C exists between the maximum temperatures predicted by the Stage Four and Five simulations. This provides an indication as to both the difficulty and importance of specifying appropriate values for the thermal boundary conditions.

The maximum temperature is still predicted to exceed 90°C, but the information provided by the fluid field would allow for the modification of the fin structure above the hottest components to most advantageously utilize the cooling flow patterns. Furthermore, flow destabilizers and turbulators could be inserted into the cavity to promote better mixing and, therefore more effective convective cooling. Also, the positions of the inlet and outlet could be adjusted to maximize the chimney effect, thereby exhausting hot fluid from, and entraining cool fluid into, the cabinet. Each of these alternatives should be evaluated before the prototype would be constructed.

Conclusions

A concurrent thermal design framework suitable for application in the design of cost-driven computer systems was described. The thermal design methodology increases in refinement with the maturity of the overall design, enabling meaningful participation in a multidisciplinary

environment. The success of such concurrent design methodologies depends upon both the accuracy and the time required to generate data. Therefore, a designer must intentionally vary the level of approximation contained within a model according to that required for resolution of a particular design objective. Furthermore, rather than attempting to optimize a specific design domain, a solution must be sought that satisfies the global design criteria. This is because of the strong interdependence among the individual design disciplines to the overall design. A seemingly small variation to satisfy a local objective may have far reaching affects upon other aspects of the total design

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Figure Captions:

Fig. 1: Schematic of one-third of the boaid.

Fig. 2: Schematic of the composition of the sample package.

Fig. 3: Plot indicating the operating point of the sample board and its packages [18]: (a) average operating point and (b) row-wise operating range.

Fig. 4: Elemental discretization of the computational domain.

Fig. 5: Schematic indicating the thermal boundary conditions.

Fig. 6: Isotherms for the Stage Two analysis: (a) rows 1-4, (b) rows 5-8, and (c) rows 9-12.

Fig. 7: Evolution of the specified row-wise heat transfer coefficient: (a) Stage Three and (b) Stage Four.

Fig. 8: Isotherms for the Stage Three analysis: (a) rows 1-4, (b) rows 5-8, and (c) rows 9-12.

Fig. 9: Isotherms for die Stage Four analysis: (a) rows 1-4, (b) rows 5-8, and (c) rows 9-12.

Fig. 10: Fully-developed flow patterns over a package: (a) velocity vectors and (b) streamlines.

Fig. 11: Instantaneous temperature field of a package in the fully developed region.

Fig. 12: Cycle-averaged local heat flux distribution.

Fig. 13: Heat transfer coefficient distribution along the board and package.

Fig. 14: Temperature distributions along the board and component based upon a T ^ ^ . , , ^ of 69.76°C using (a) conduction-only simulation and (b) conjugate conduction/convection simulation.

Fig. 15: Schematic of the Vu-Man.

Fig. 16: Stage Four analysis of the Vu-Man's lower board.

Fig. 17: Stage Five analysis of the Vu-Man: (a) velocity field and (b) thermal field.

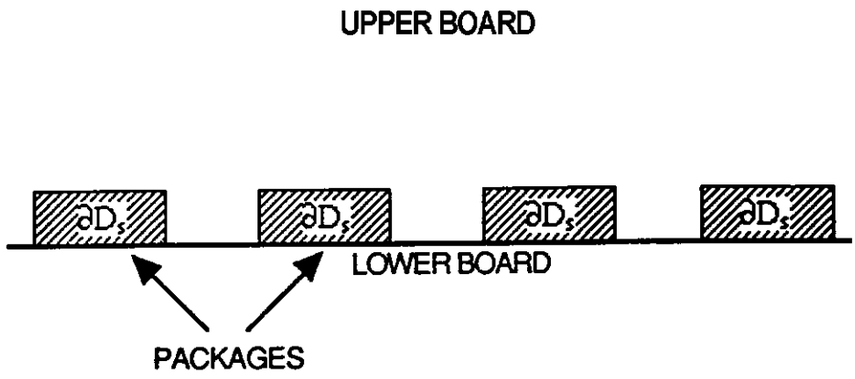

UPPER BOARD
∂D_s
∂D_s
∂D_s
∂D_s
LOWER BOARD
PACKAGES

Fig. 1

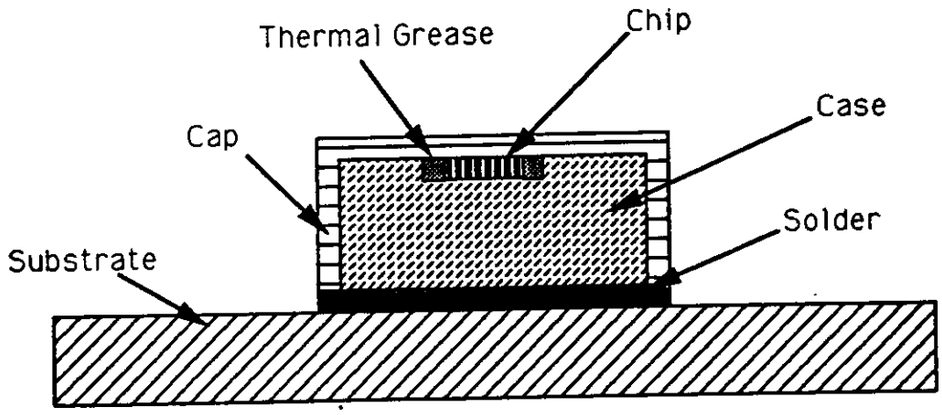
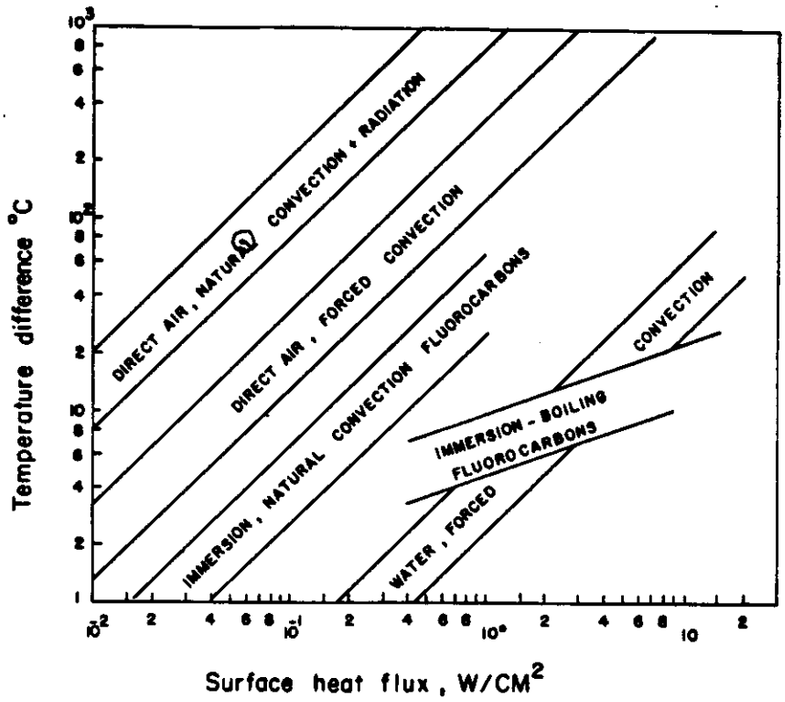
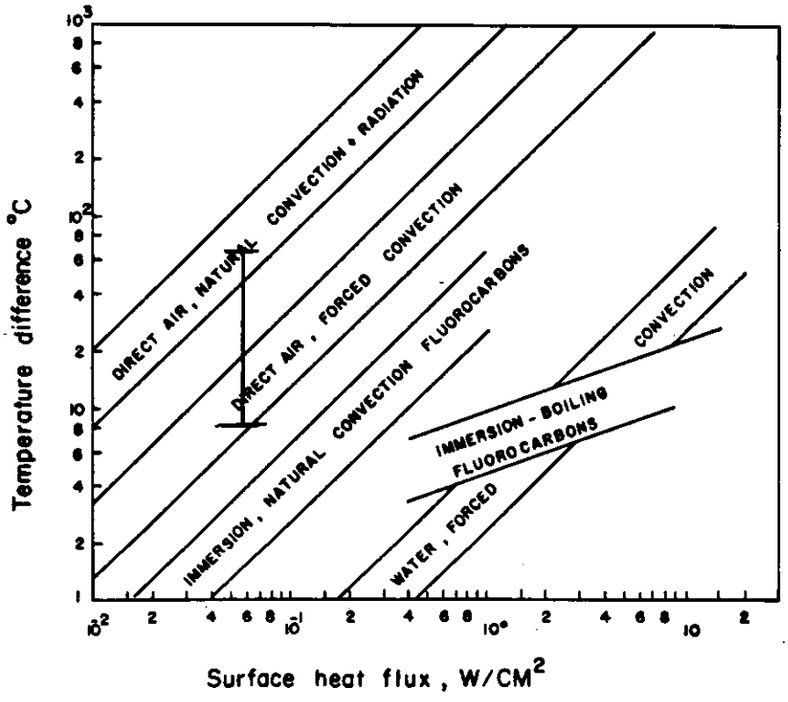

Thermal Grease
Chip
Case
Cap
Solder
Substrate

Fig. 2


Temperature difference °C
DIRECT AIR, NATURAL CONVECTION + RADIATION
DIRECT AIR, FORCED CONVECTION
IMMERSION, NATURAL CONVECTION FLUOROCARBONS
IMMERSION - BOILING FLUOROCARBONS
CONVECTION
WATER, FORCED
Surface heat flux, W/CM²

(a)


Temperature difference °C
DIRECT AIR, NATURAL CONVECTION + RADIATION
DIRECT AIR, FORCED CONVECTION
IMMERSION, NATURAL CONVECTION FLUOROCARBONS
IMMERSION - BOILING FLUOROCARBONS
CONVECTION
WATER, FORCED
Surface heat flux, W/CM²

(b)

Fig. 3

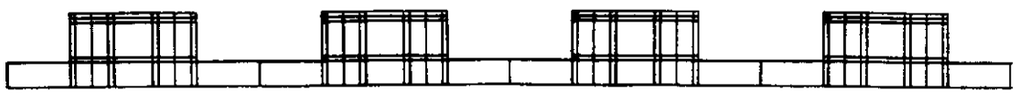


Fig. 4

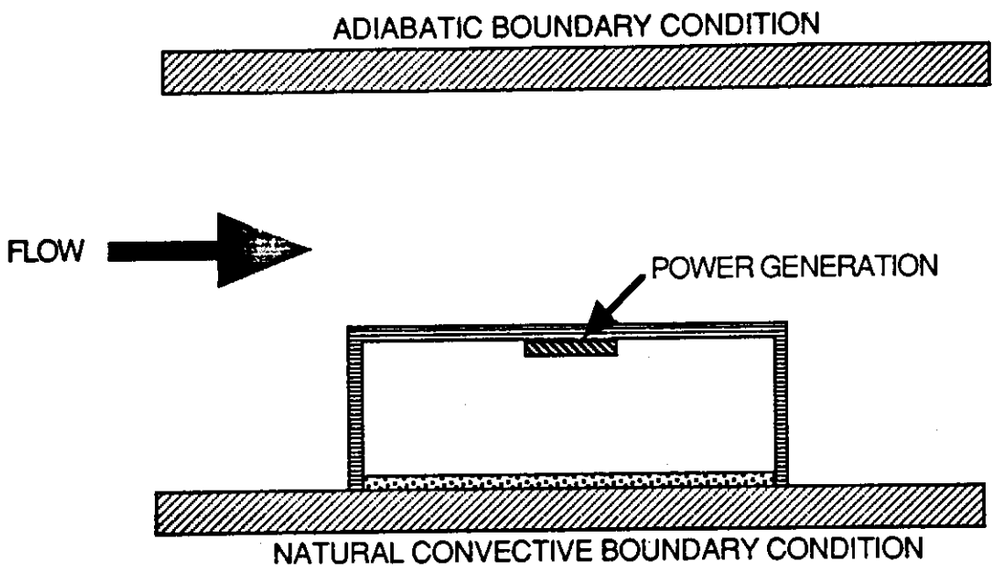
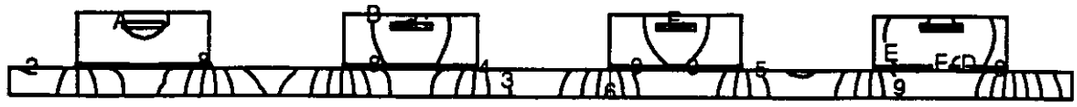

ADIABATIC BOUNDARY CONDITION
FLOW
POWER GENERATION
NATURAL CONVECTIVE BOUNDARY CONDITION

Fig. 5



(a)

Level	Temp
F	58.70
E	57.67
D	56.64
C	55.60
B	54.57
A	53.53
9	52.50
8	51.47
7	50.43
6	49.40
5	48.37
4	47.33
3	46.30
2	45.26
1	44.23

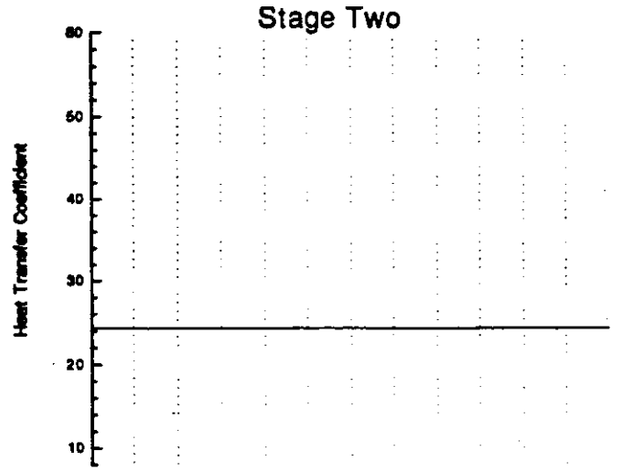
(b)

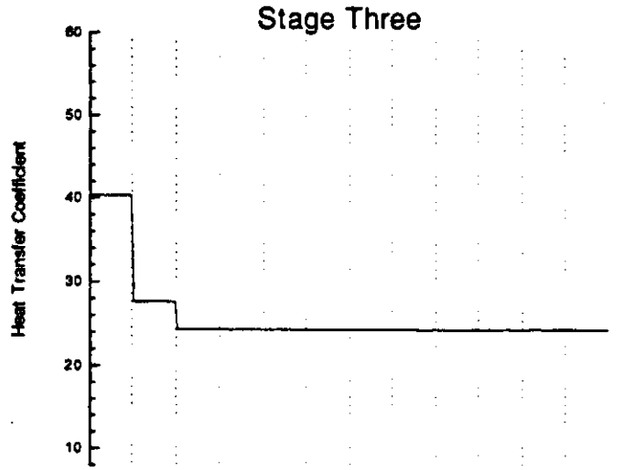
Level	Temp
F	67.48
E	66.44
D	65.40
C	64.37
B	63.33
A	62.30
9	61.26
8	60.22
7	59.19
6	58.15
5	57.11
4	56.08
3	55.04
2	54.01
1	52.97

(c)

Level	Temp
F	76.25
E	75.21
D	74.17
C	73.13
B	72.10
A	71.06
9	70.02
8	68.98
7	67.94
6	66.90
5	65.86
4	64.83
3	63.79
2	62.75
1	61.71

Fig. 6


Stage Two
Heat Transfer Coefficient
60
50
40
30
20
10


Stage Three
Heat Transfer Coefficient
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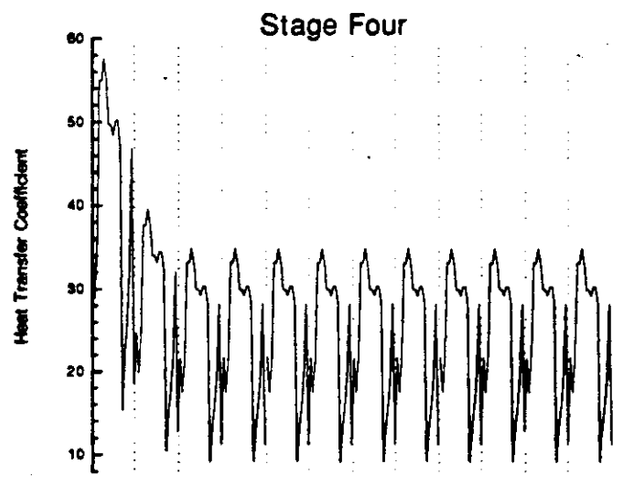
50
40
30
20
10


Stage Four
Heat Transfer Coefficient
60
50
40
30
20
10

(a)

Level	Temp
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E	56.20
D	54.84
C	53.49
B	52.13
A	50.78
9	49.42
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7	46.71
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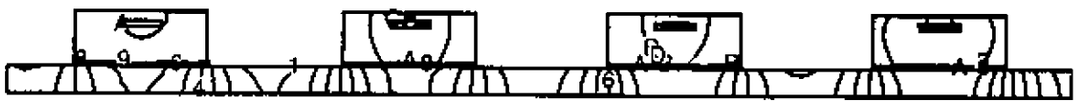
5	44.00
4	42.65
3	41.29
2	39.93
1	38.58



(b)

Level	Temp
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E	66.44
D	65.40
C	64.37
B	63.33
A	62.30
9	61.26
8	60.22
7	59.19
6	58.15
5	57.11
4	56.08
3	55.04
2	54.01
1	52.97

(c)

Level	Temp
F	76.25
E	75.21
D	74.17
C	73.13
B	72.10
A	71.06
9	70.02
8	68.98
7	67.94
6	66.90
5	65.86
4	64.83
3	63.79
2	62.75
1	61.71

Fig. 8

(a)

Level	Temp
F	58.33
E	57.14
D	55.94
C	54.75
B	53.55
A	52.36
9	51.17
8	49.97
7	48.78
6	47.58
5	46.39
4	45.20
3	44.00
2	42.81
1	41.61

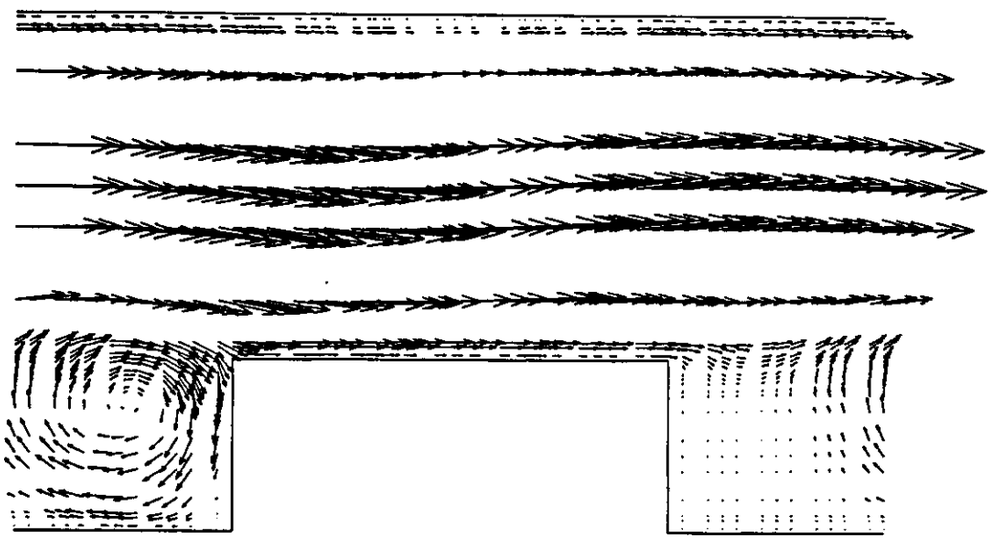
(b)

Level	Temp
F	68.46
E	67.58
D	66.70
C	65.81
B	64.93
A	64.04
9	63.16
8	62.27
7	61.39
6	60.51
5	59.62
4	58.74
3	57.85
2	56.97
1	56.08

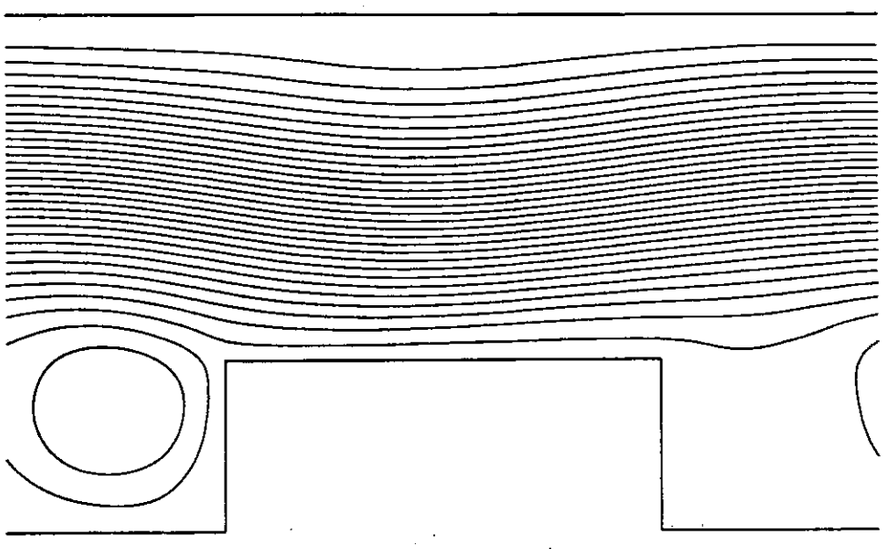
(c)

Level	Temp
F	77.21
E	76.32
D	75.43
C	74.54
B	73.65
A	72.75
9	71.86
8	70.97
7	70.08
6	69.19
5	68.30
4	67.40
3	66.51
2	65.62
1	64.73

Fig. 9

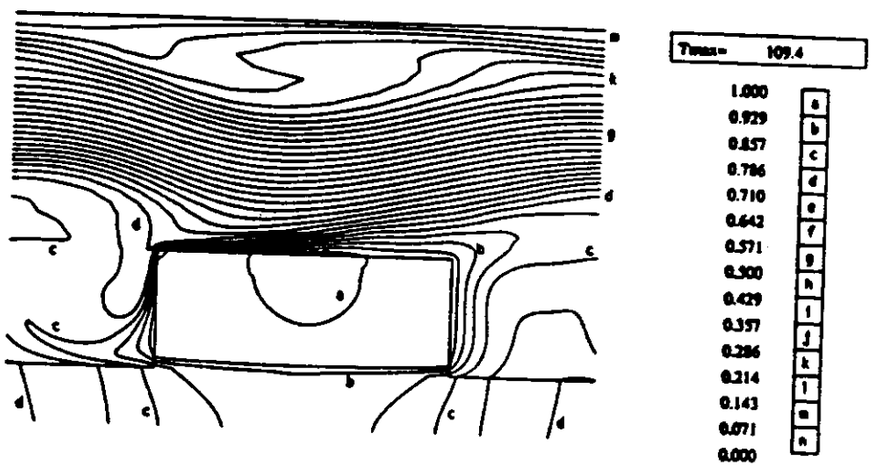


(a)



(b)

Fig. 10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0.710
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0.571
0.500
0.429
0.357
0.286
0.214
0.143
0.071
0.000

Fig. 11

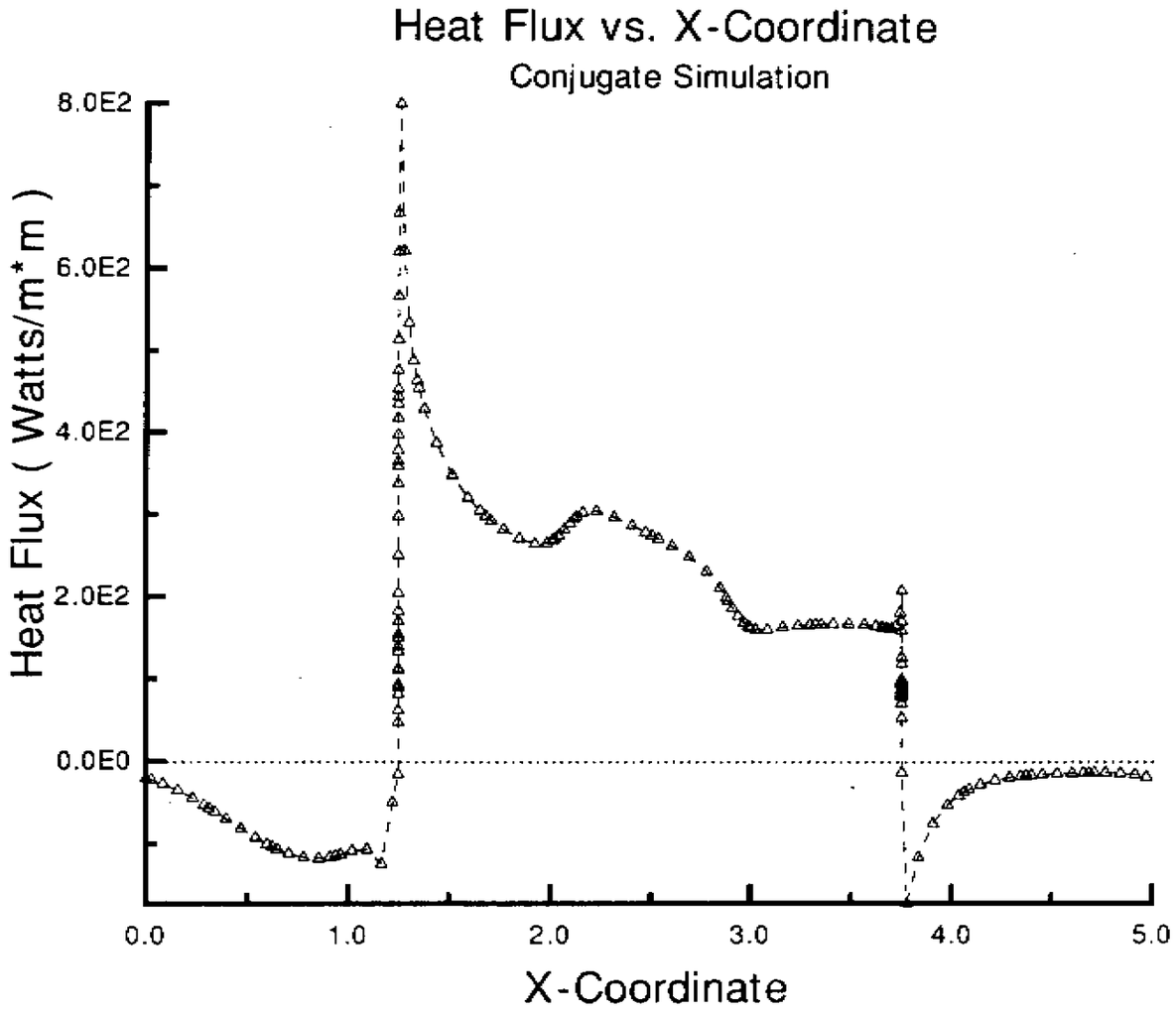

Heat Flux vs. X-Coordinate
Conjugate Simulation
Heat Flux (Watts/m*m)
8.0E2
6.0E2
4.0E2
2.0E2
0.0E0
0.0
1.0
2.0
3.0
4.0
5.0
X-Coordinate

Fig. 12

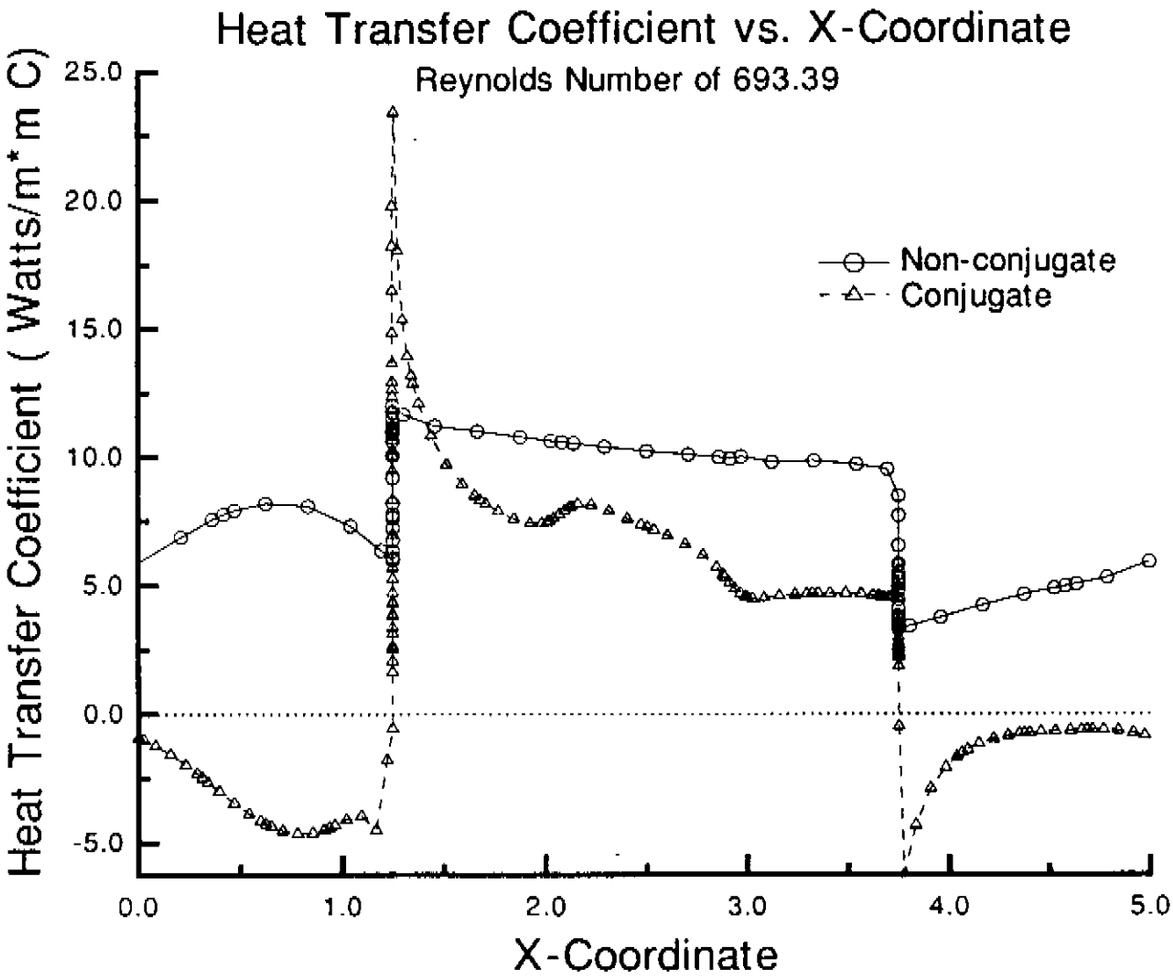
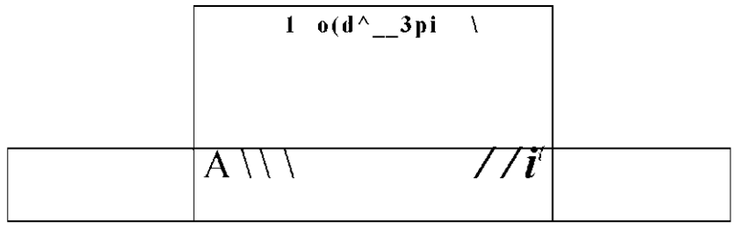

Heat Transfer Coefficient vs. X-Coordinate
Reynolds Number of 693.39
Heat Transfer Coefficient (Watts/m*m C)
25.0
20.0
15.0
10.0
5.0
0.0
-5.0
0.0
1.0
2.0
3.0
4.0
5.0
X-Coordinate
Non-conjugate
Conjugate

Fig. 13



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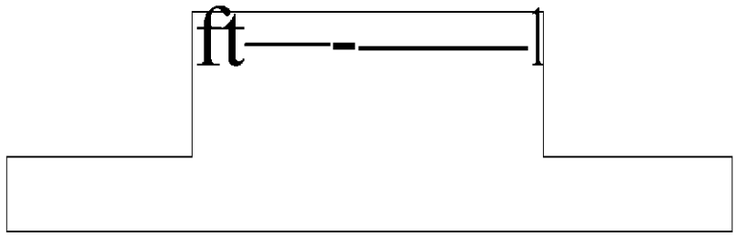
1=86.36

(a)



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4=95.72
1=93.25

(b)

Fig. 14

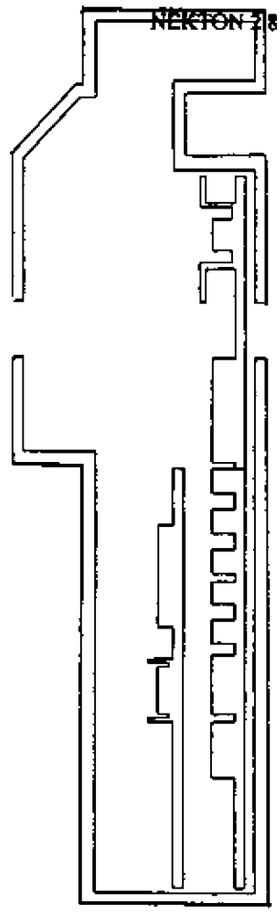
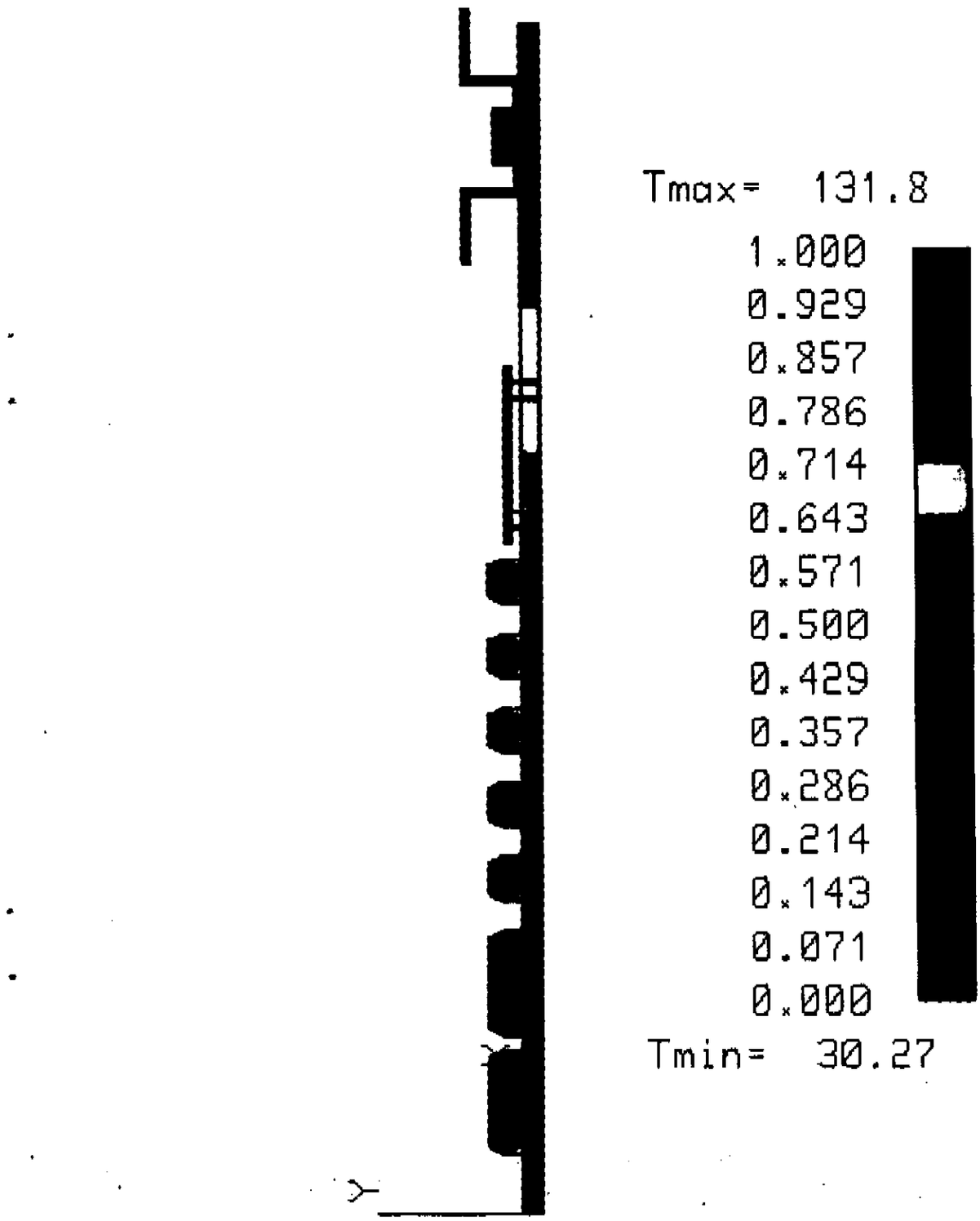


Fig. 15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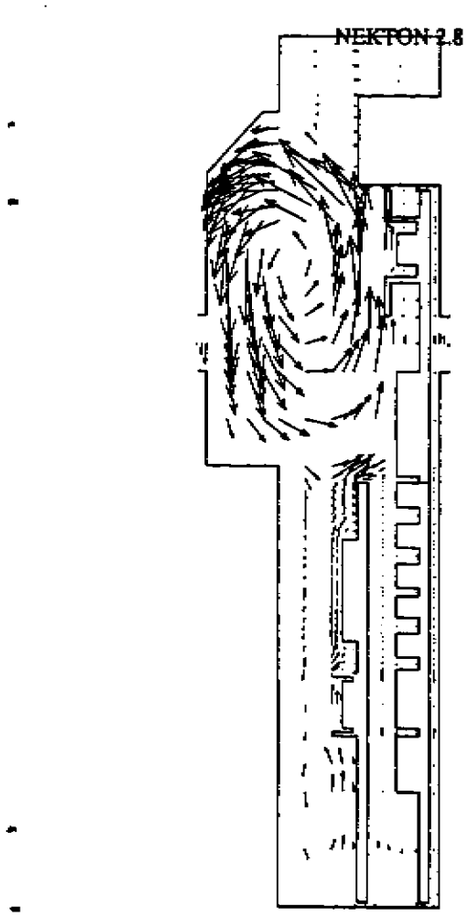
0.214
0.143
0.071
0.000
Tmin= 30.27

Fig. 16



(a)

(b)

Fig. 17