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CMU-11 ENGINEERING DOCUMENTATION

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Pittsburgh, PA 15213

January 1977

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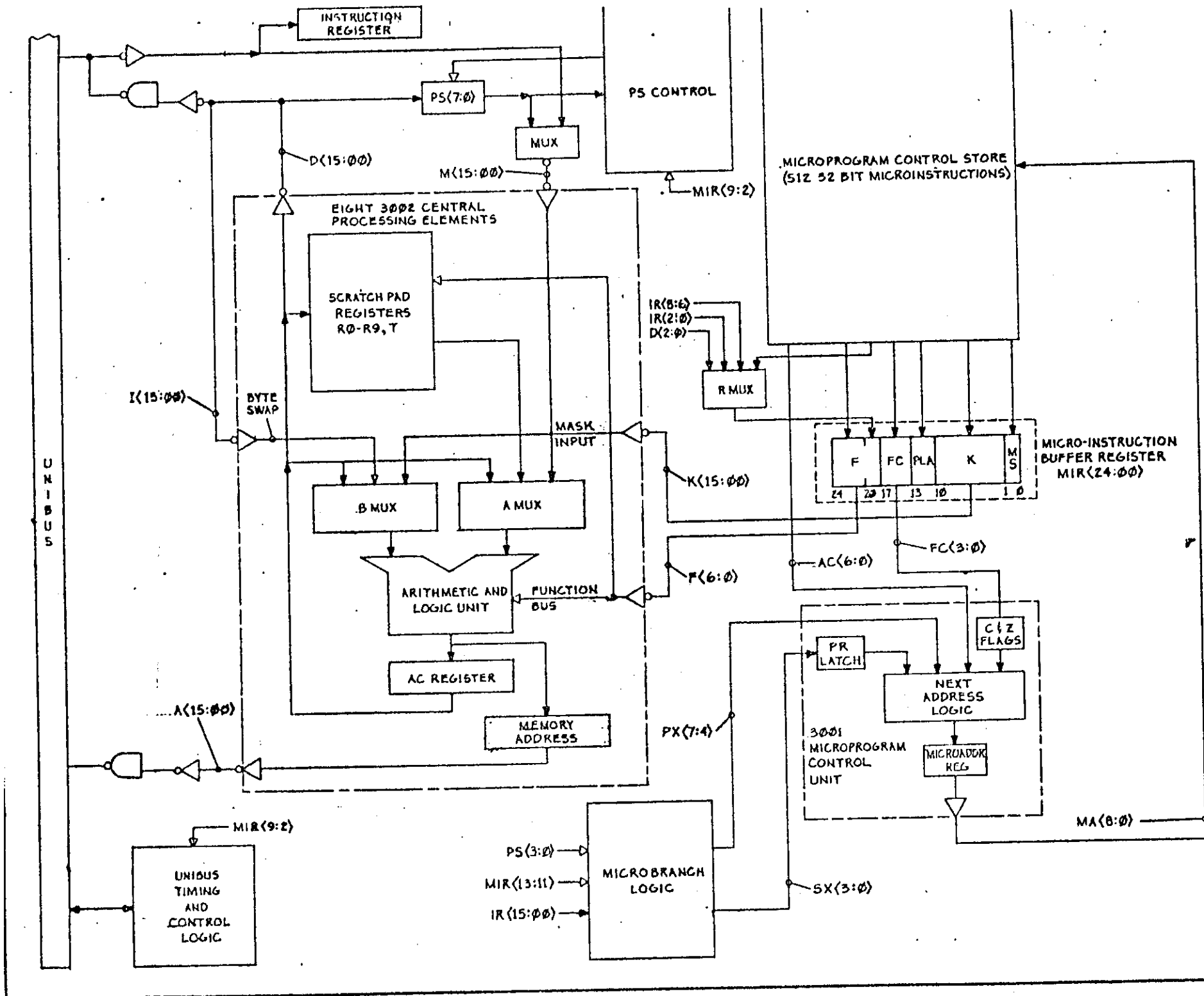
ABSTRACT

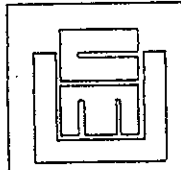
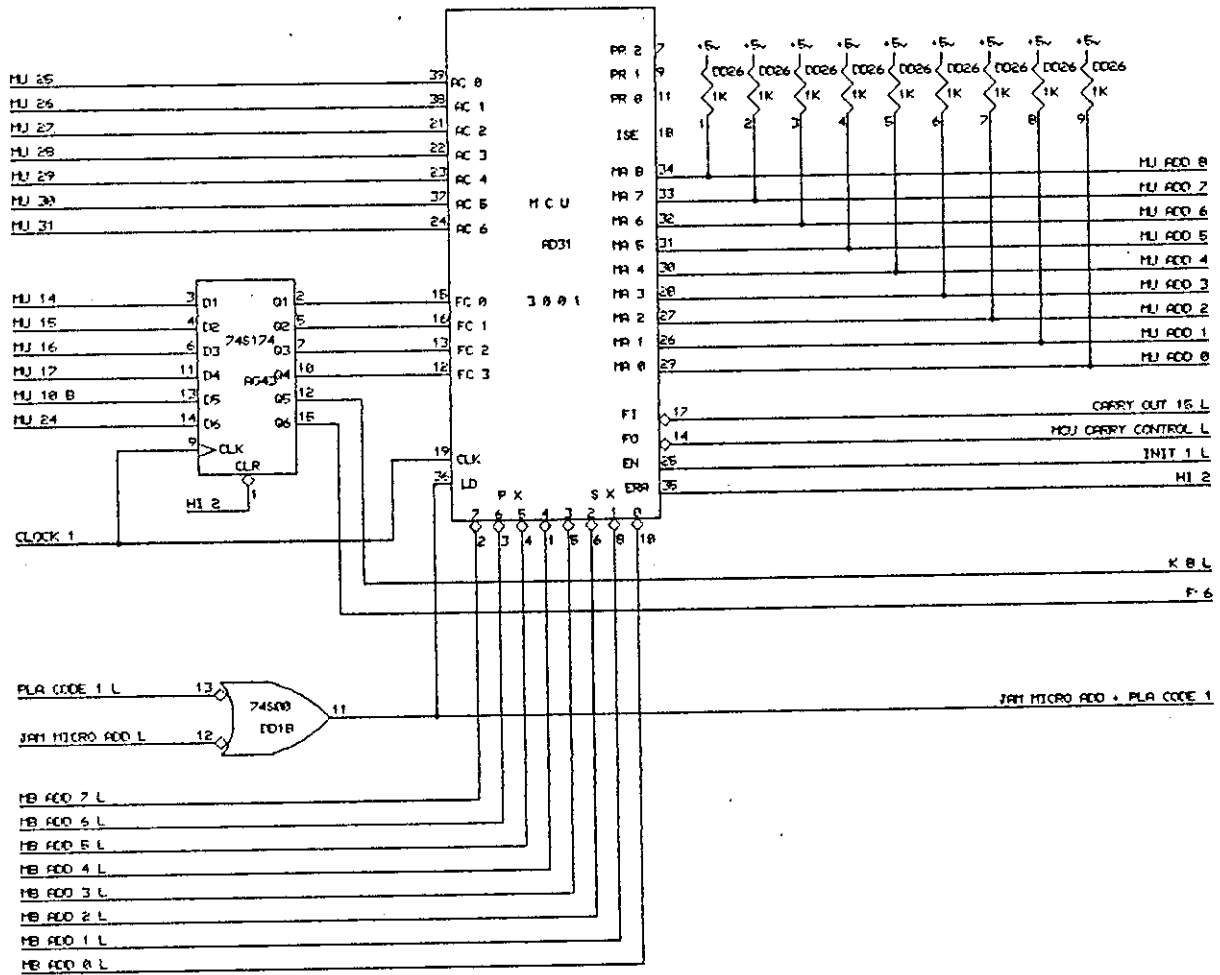
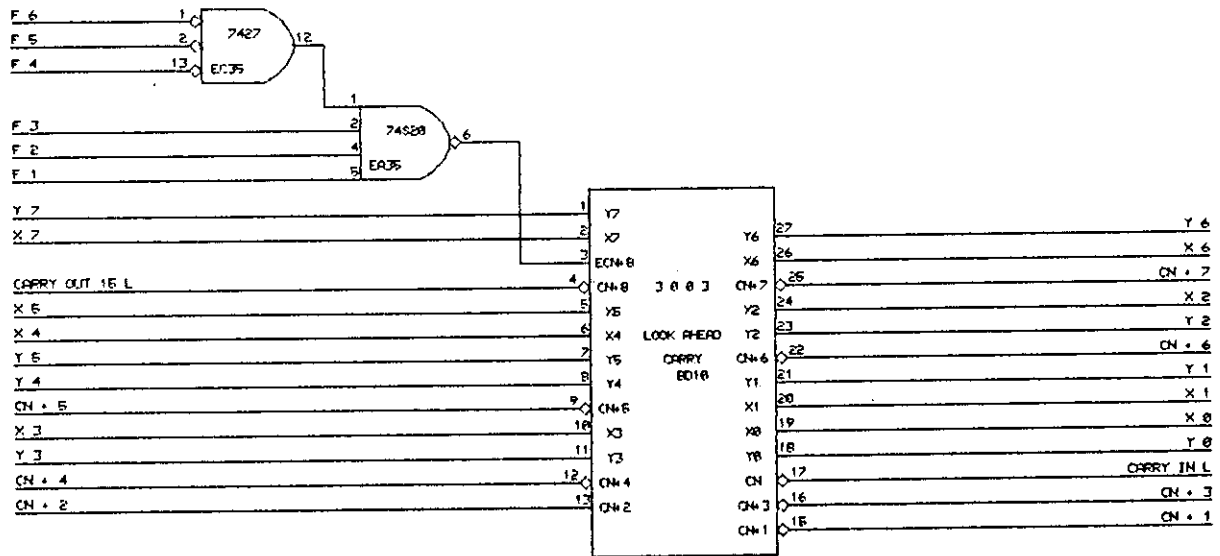
The CMU-11 is a microprogrammable processor built with the Intel 3000 microcomputer set that emulates the PDP-11 architecture. In addition, it has been designed to provide full Unibus support. The enclosed documentation gives the details of the CMU-11 design. This documentation has been generated in conjunction with the Stanford Drawing System, the SAGE simulator, and the Intel 3000 microassembler. Those hoping to do any further development of the CMU-11 design are encouraged to also use these design aids and all of the CMU-11 design information shown here (and other information such as ROM contents and wirelists) are available on magnetic tape. See the following report for an introductory discussion and evaluation of the CMU-11:

McWilliams, T. M., S. H. Fuller, and W. H. Sherwood, "Using LSI Processor Bit-Slice to Build a PDP-11: A Case Study in Microcomputer Design," Technical Report, Department of Computer Science, Carnegie-Mellon University, Pittsburgh, PA, January 1976.

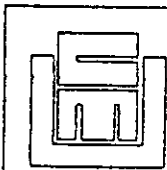
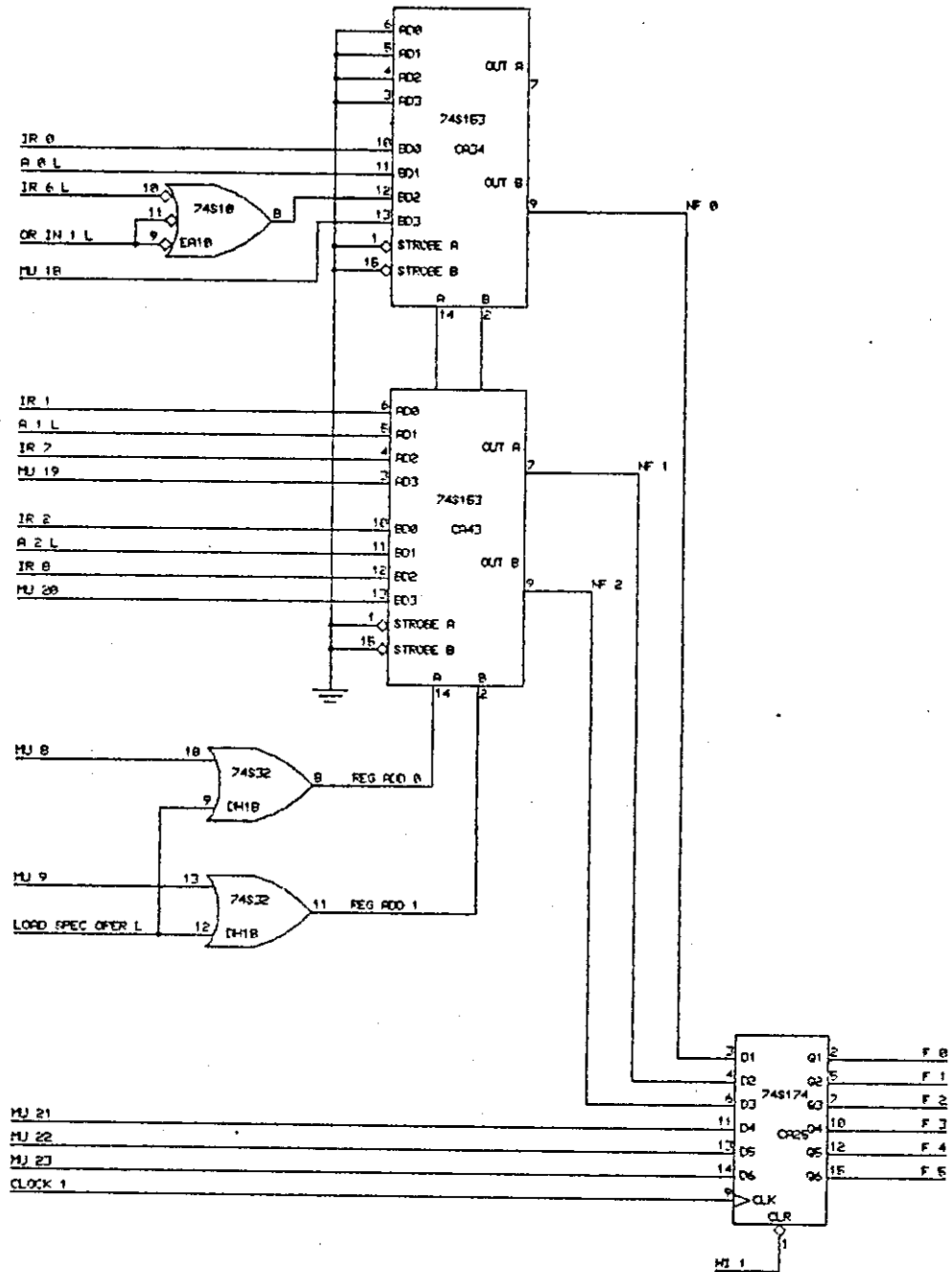
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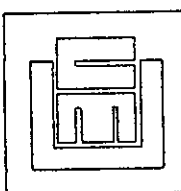
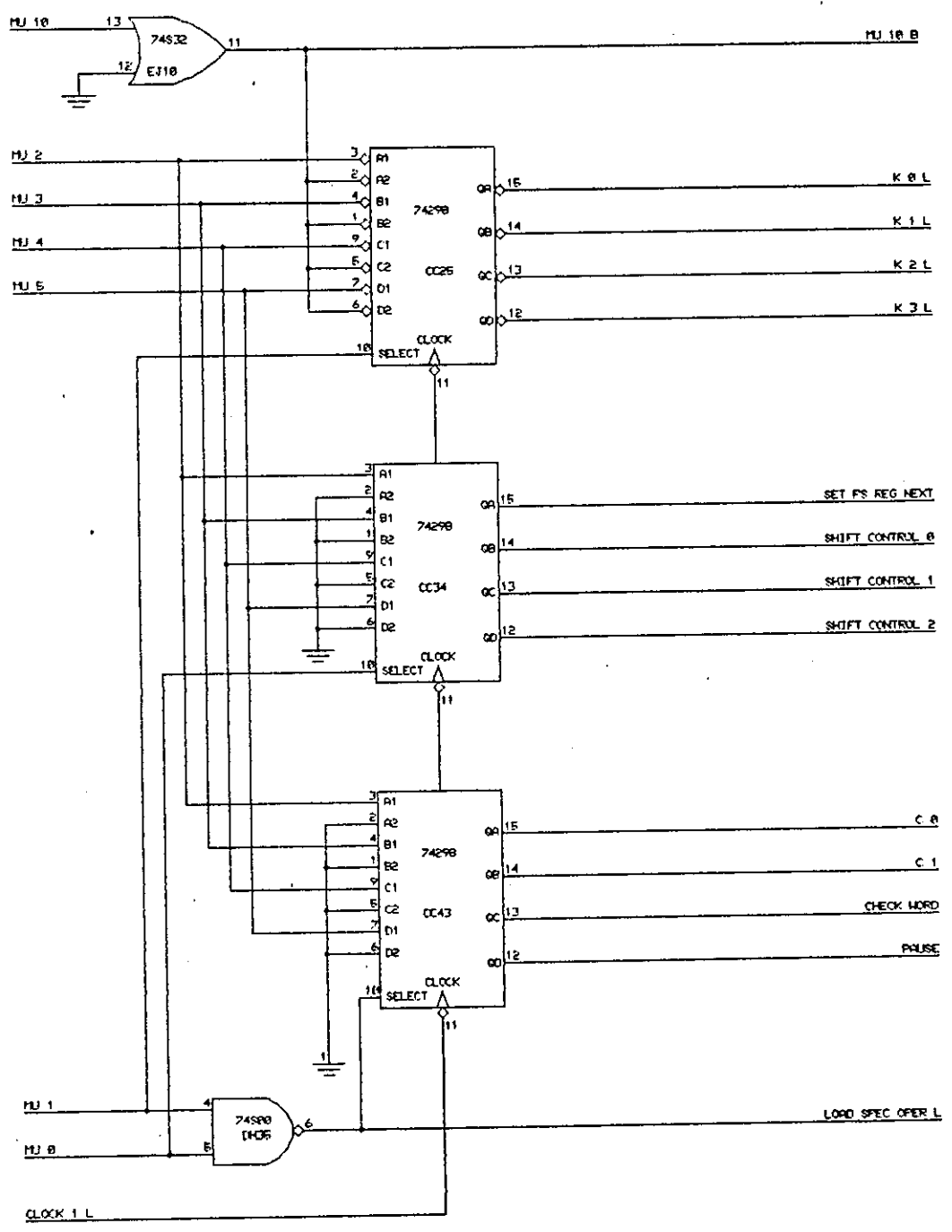




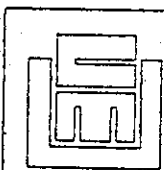
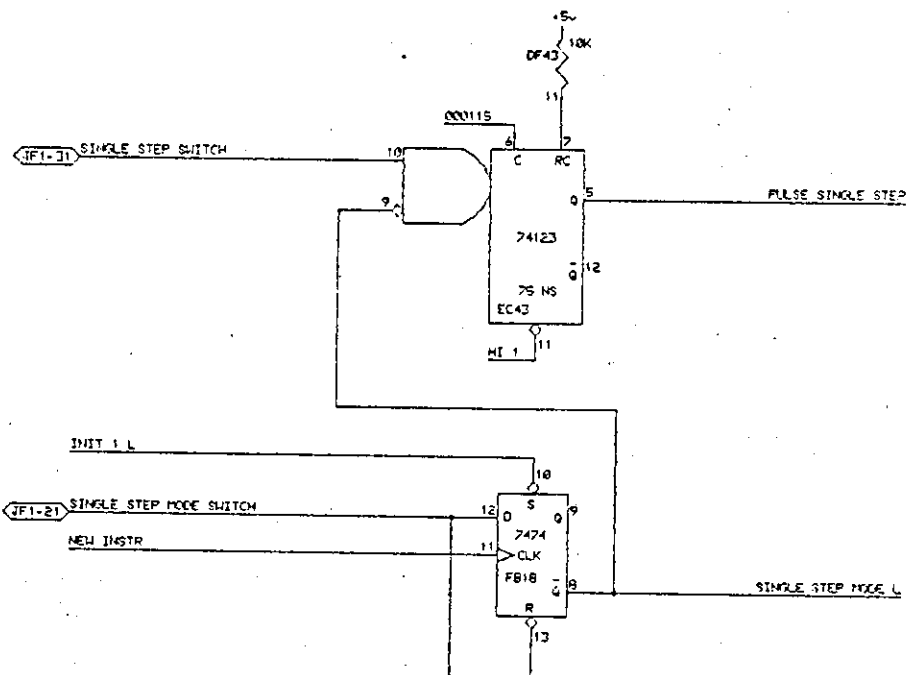
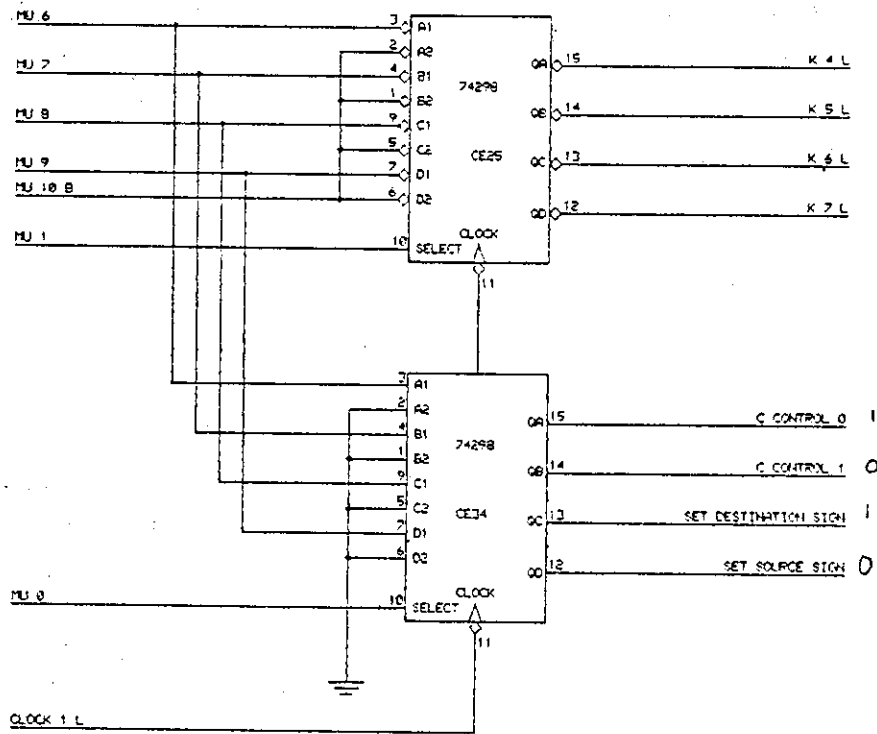
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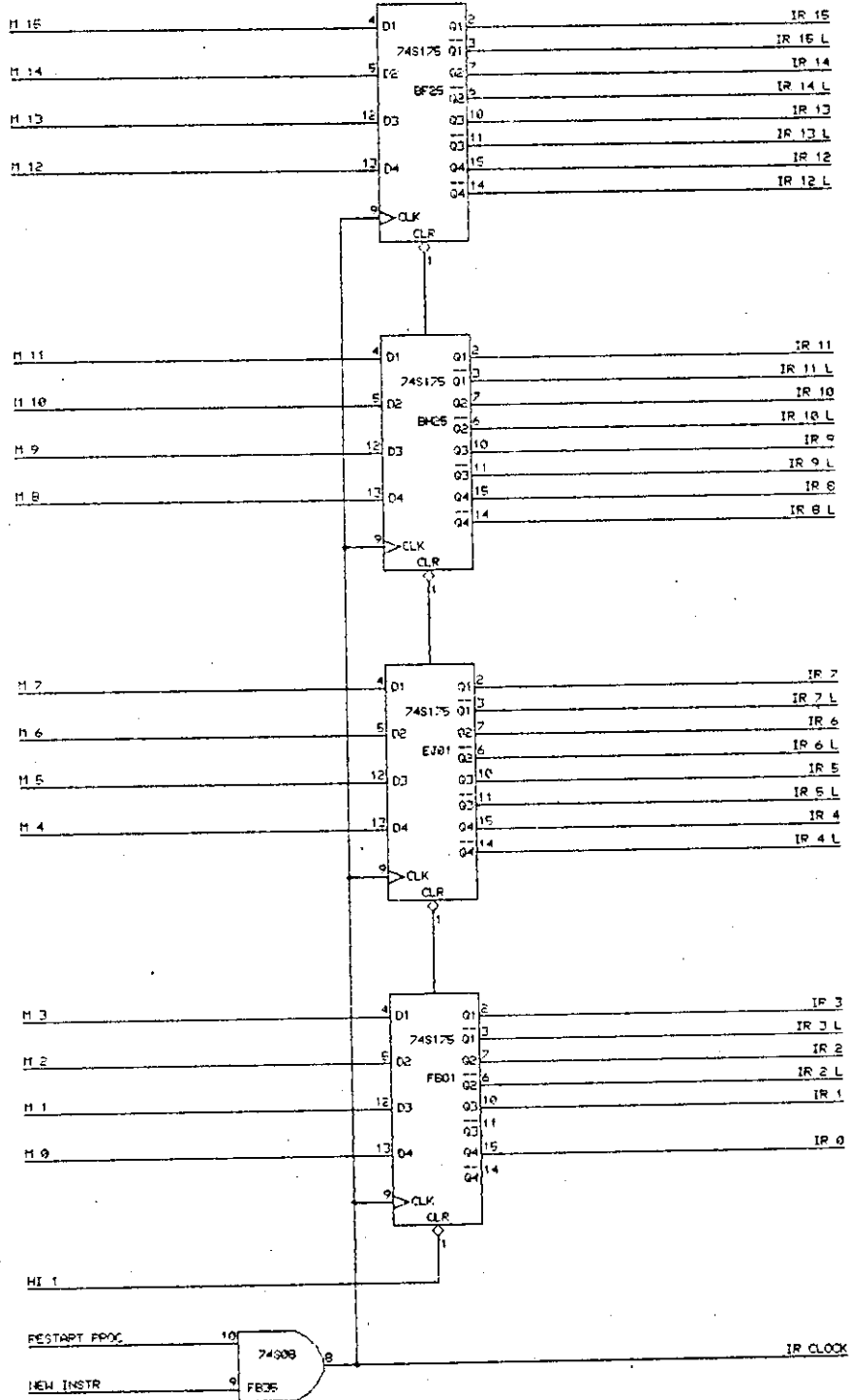
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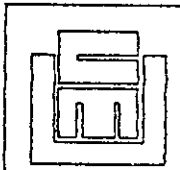
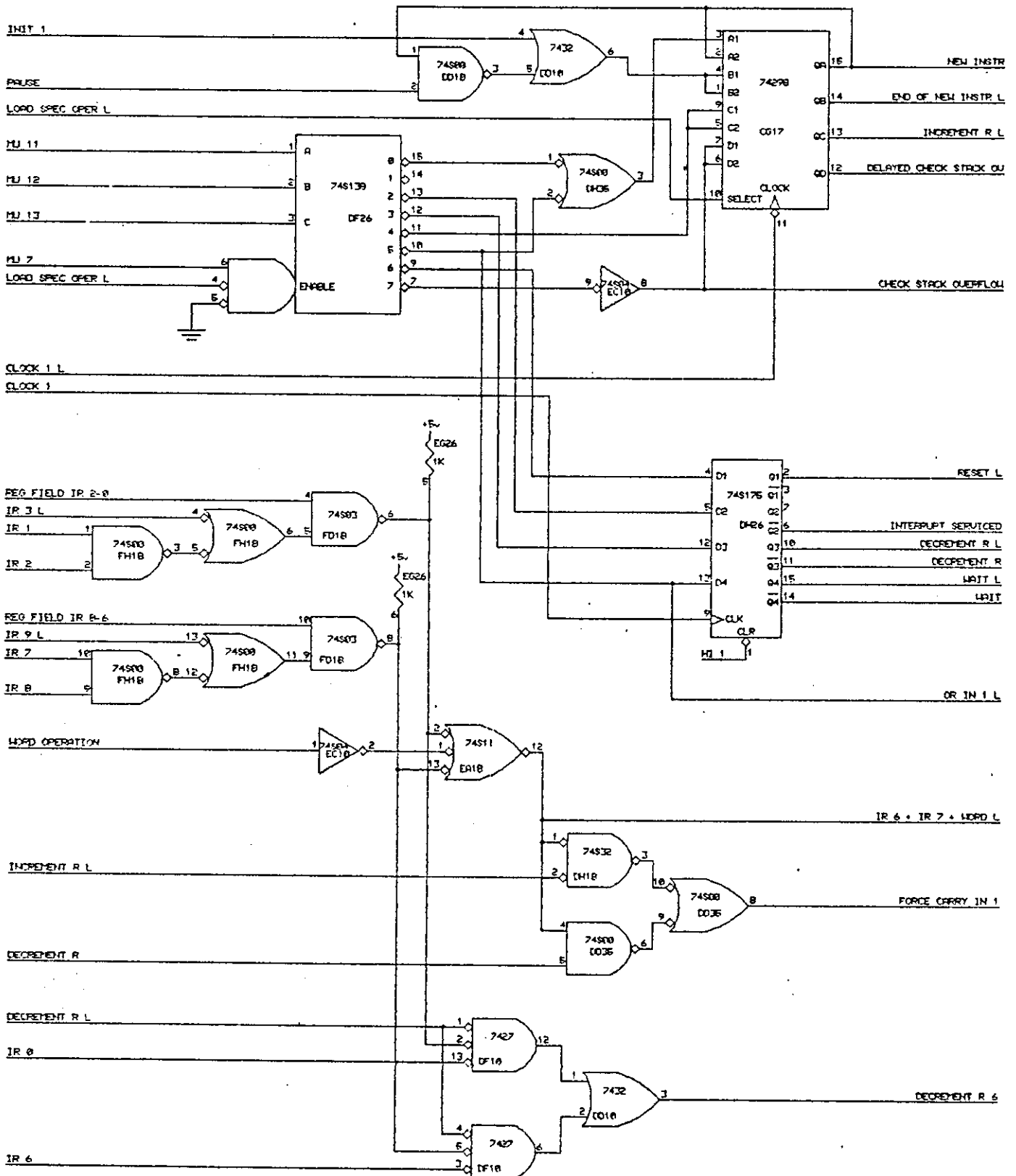
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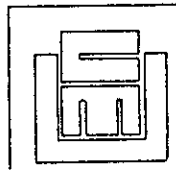
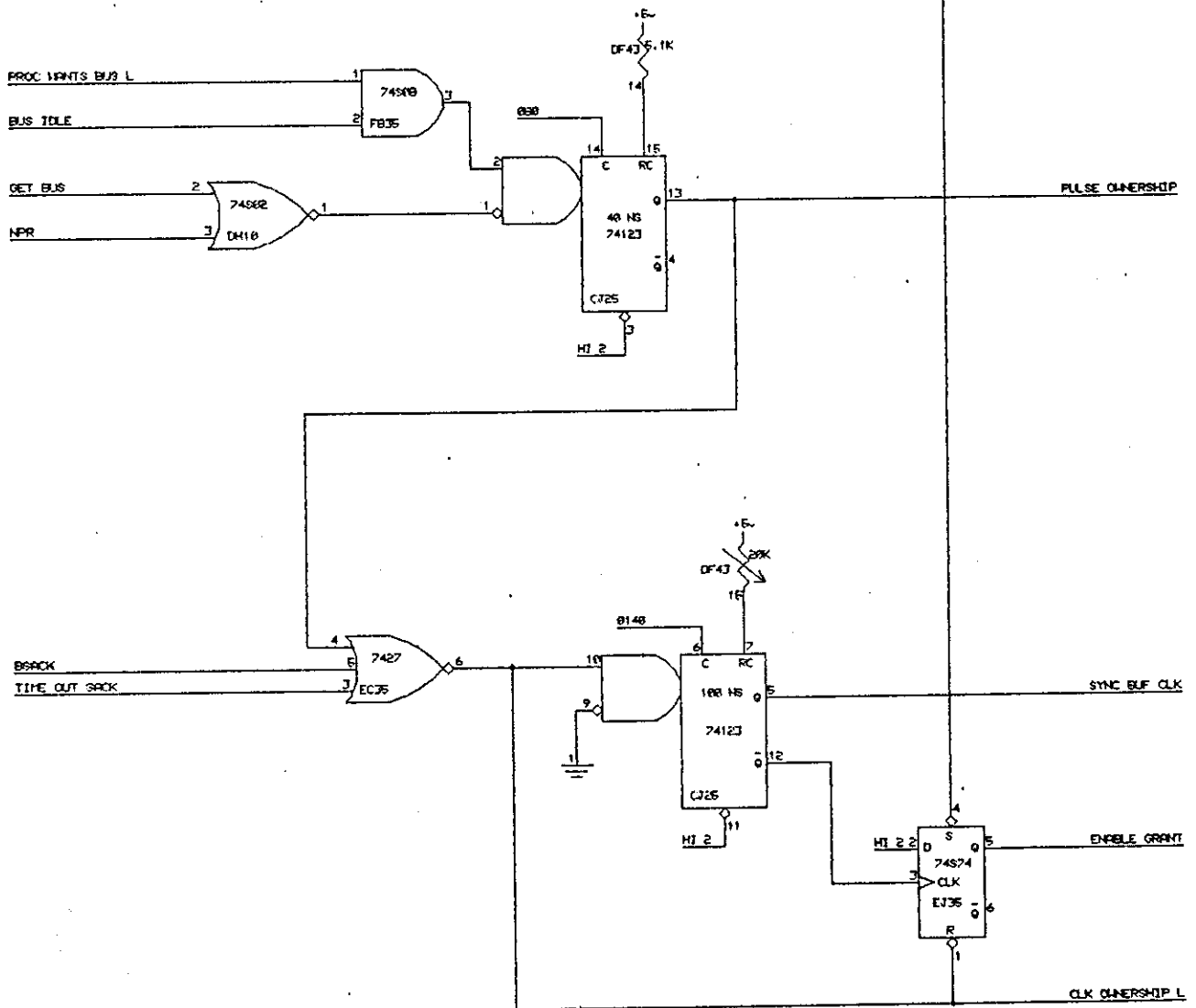


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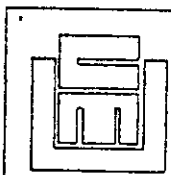
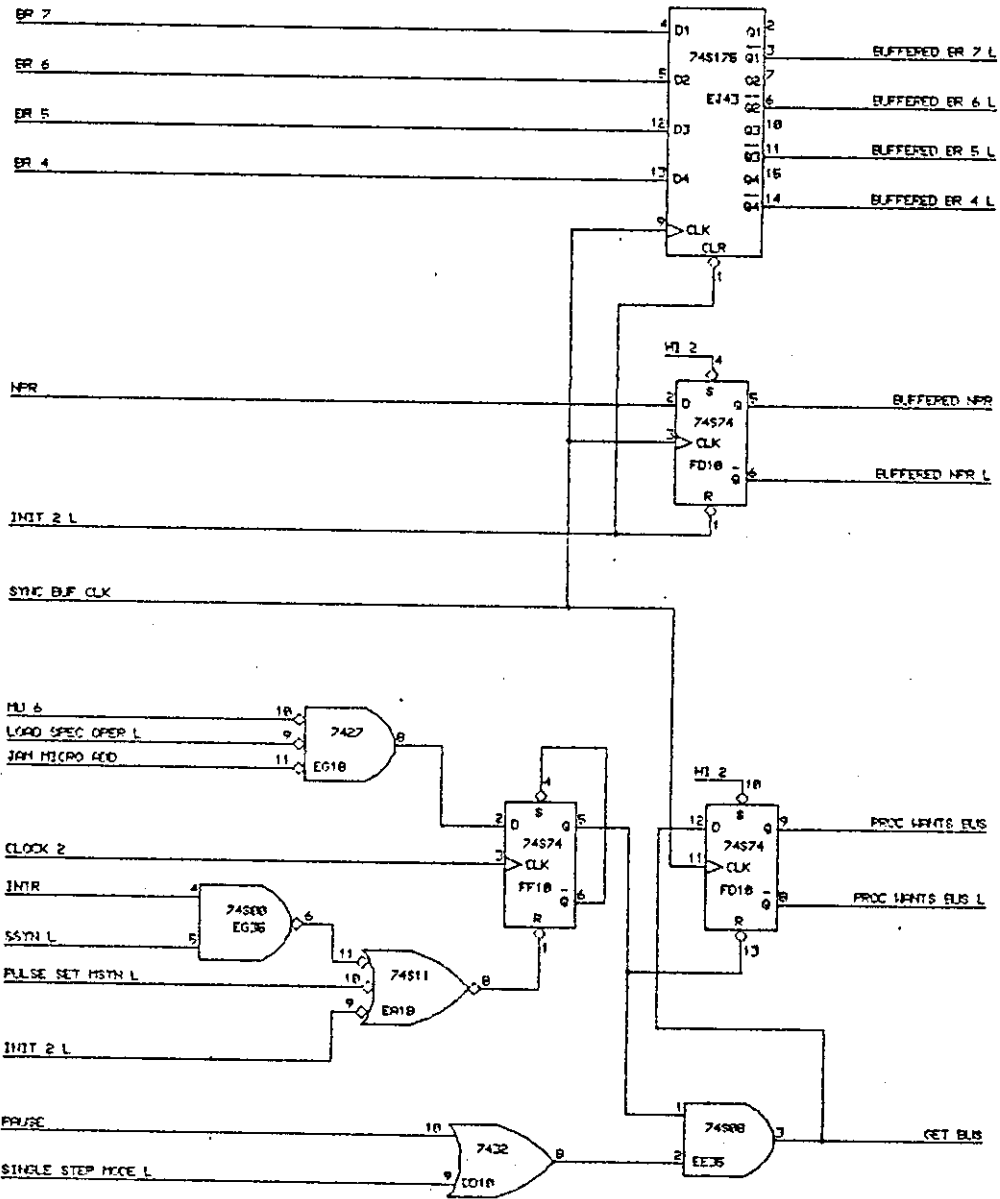


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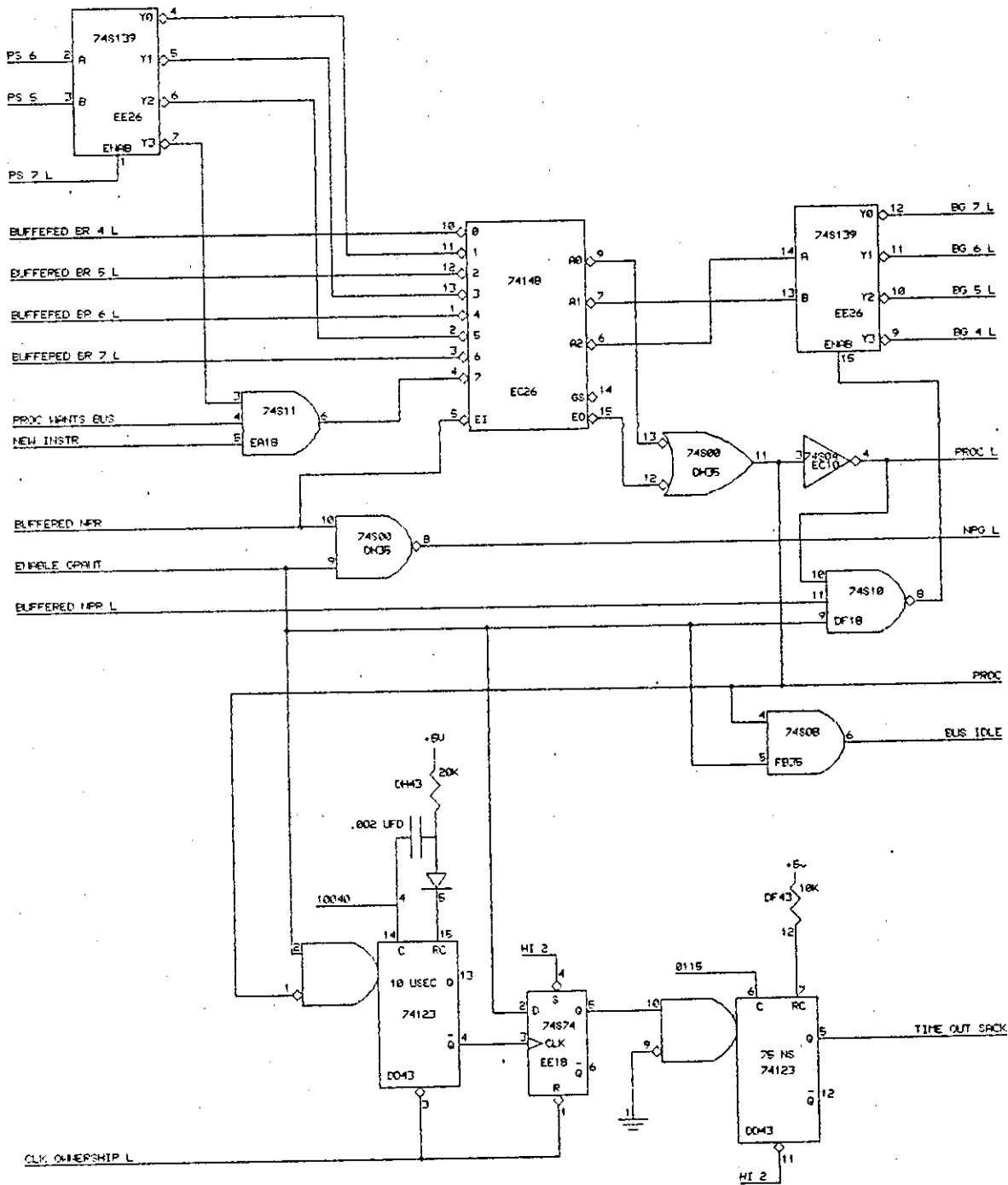
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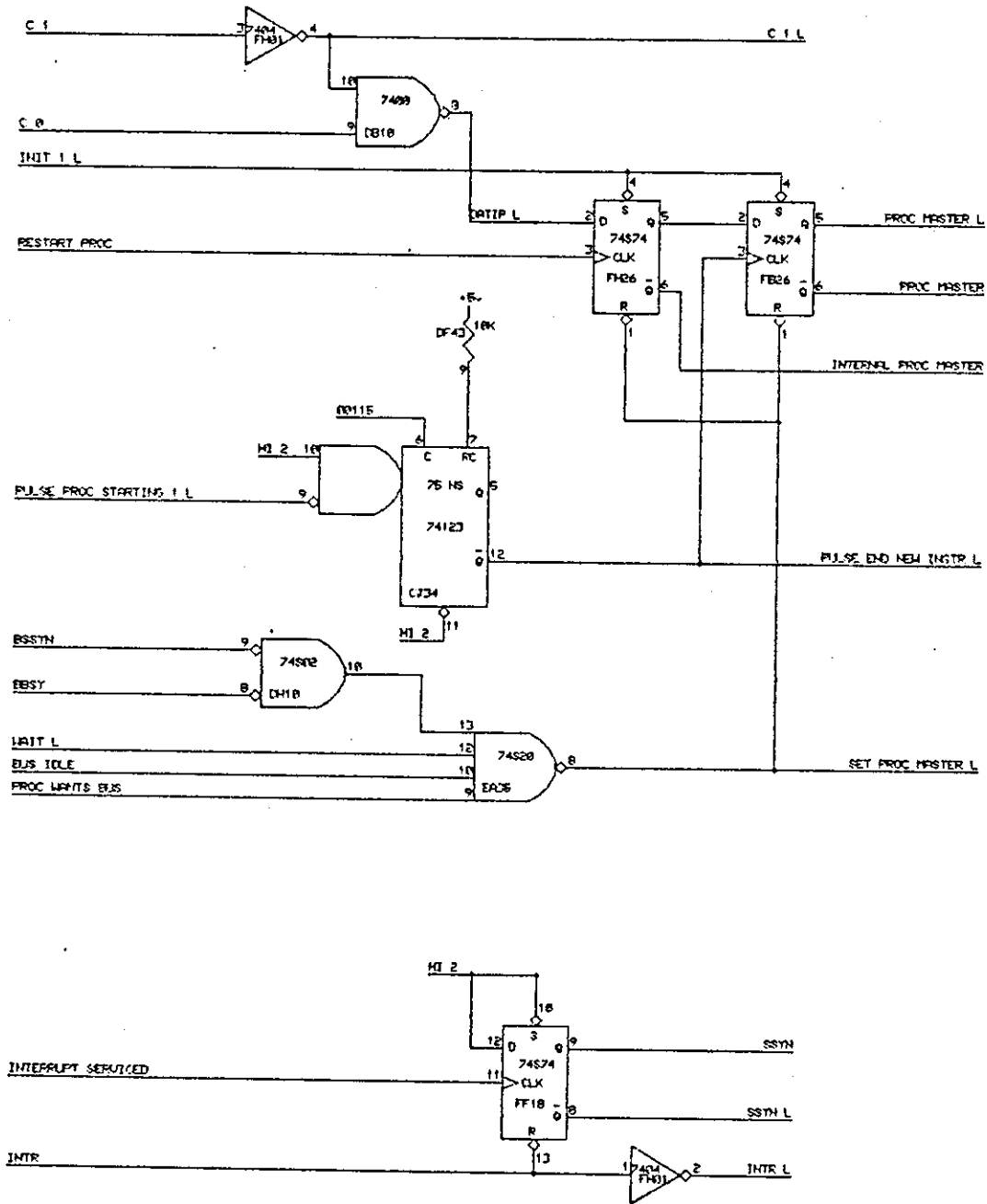
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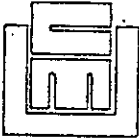


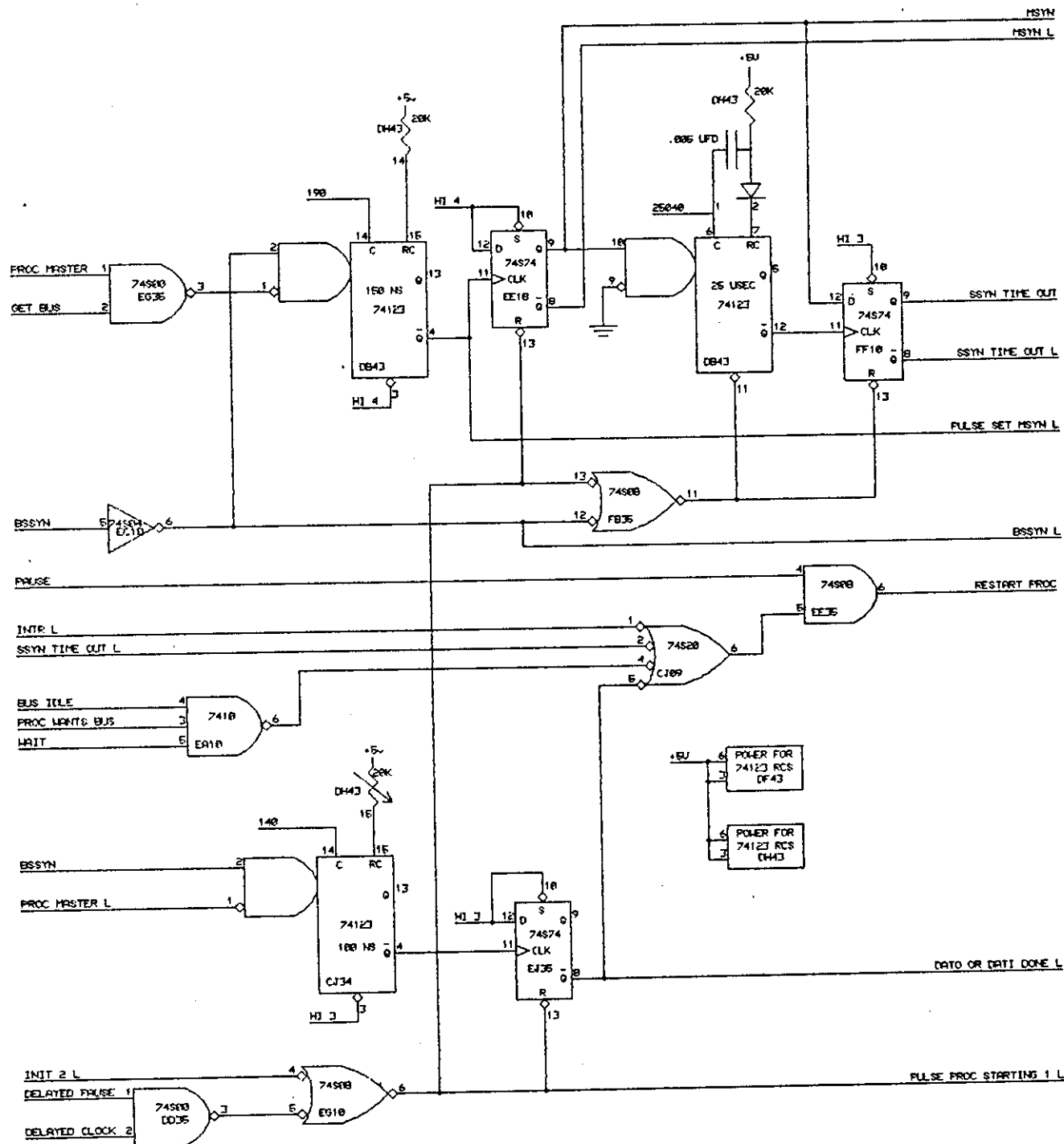
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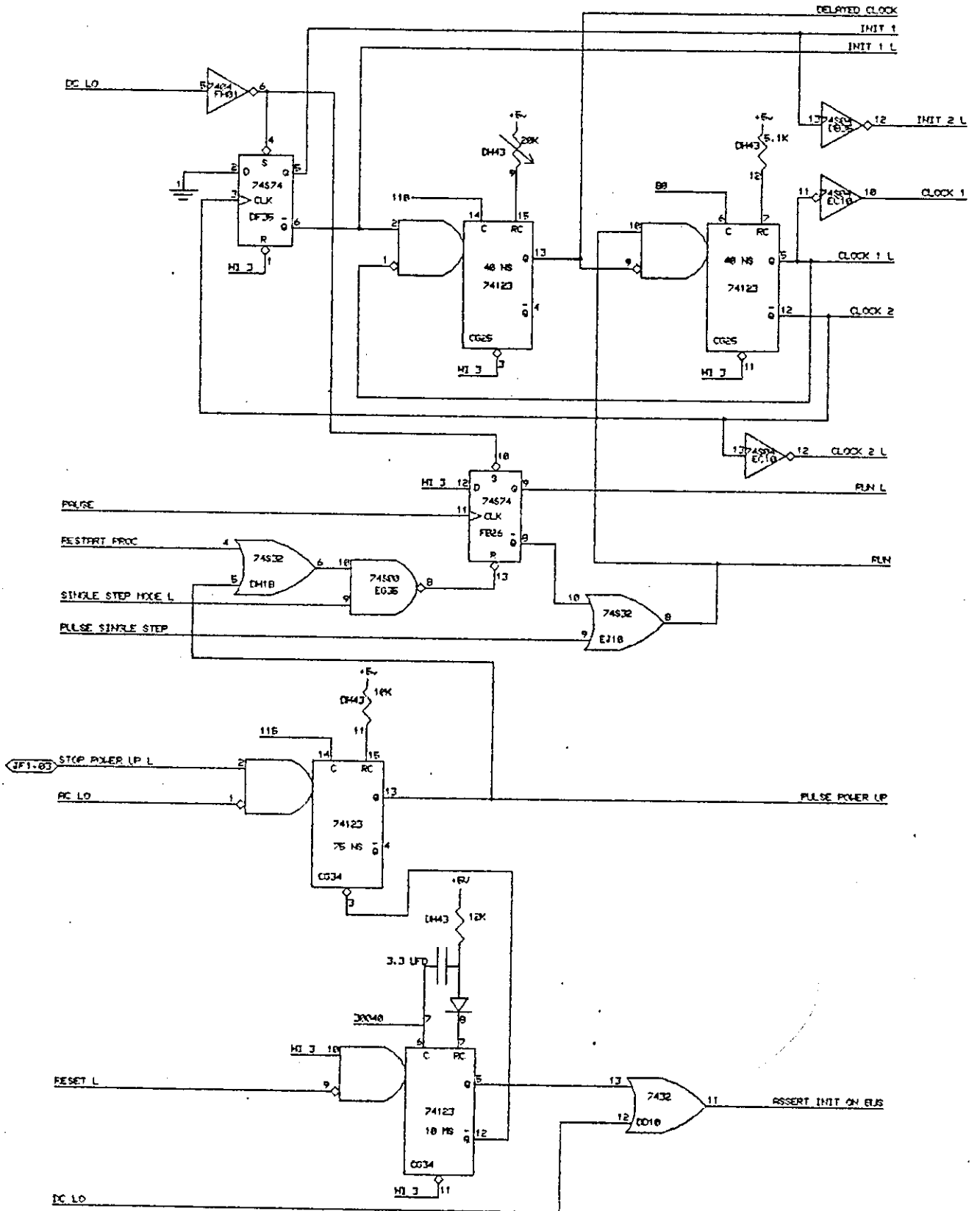


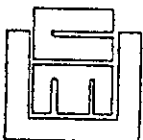
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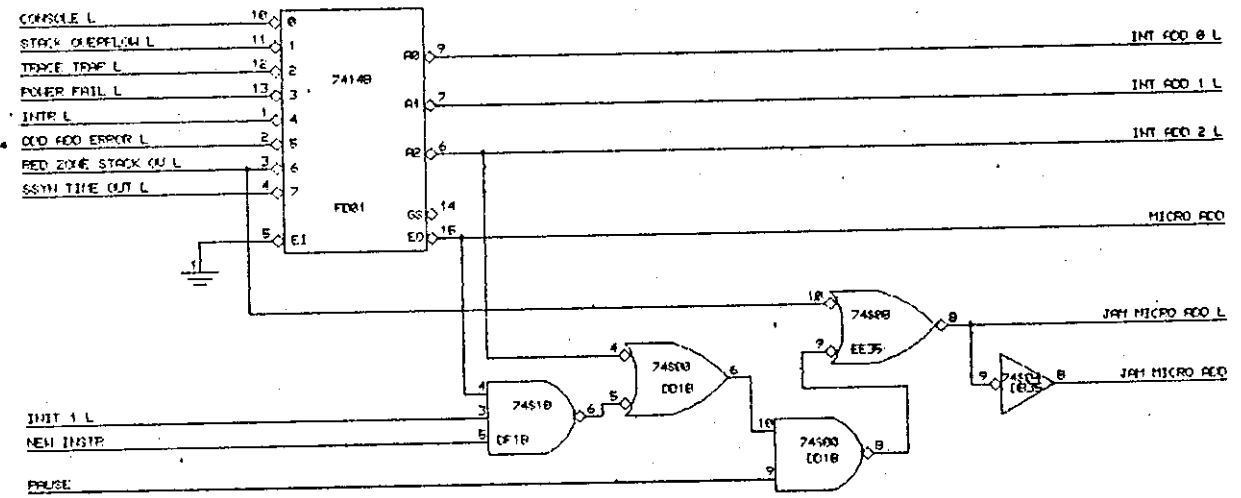
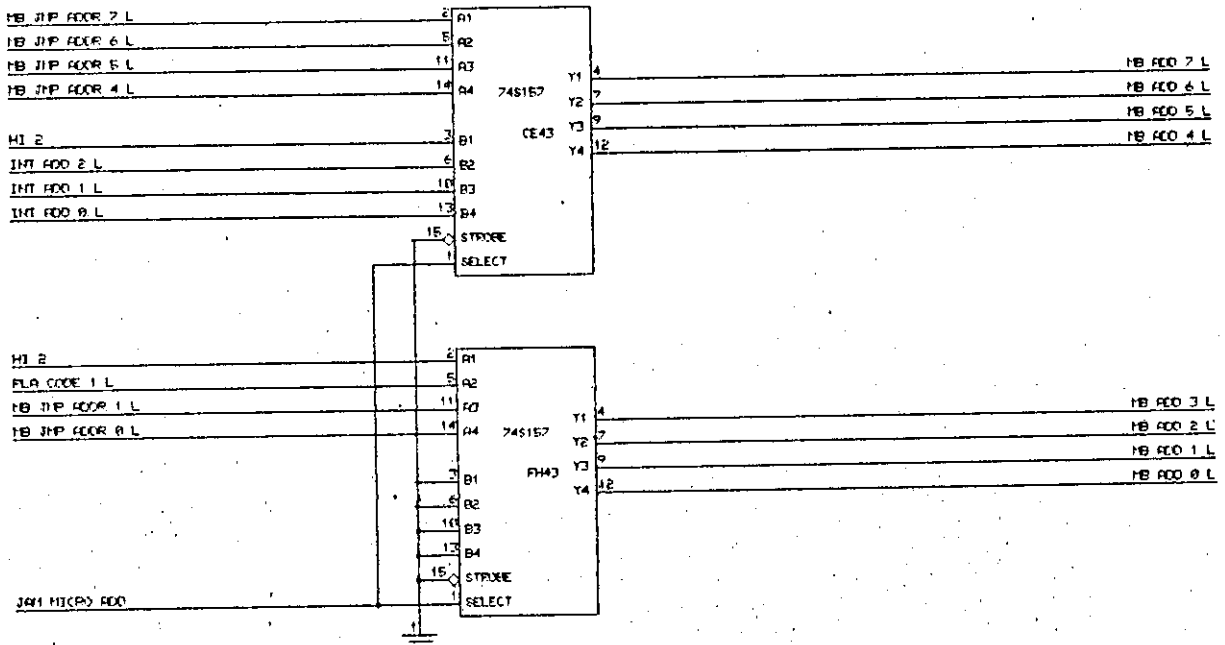


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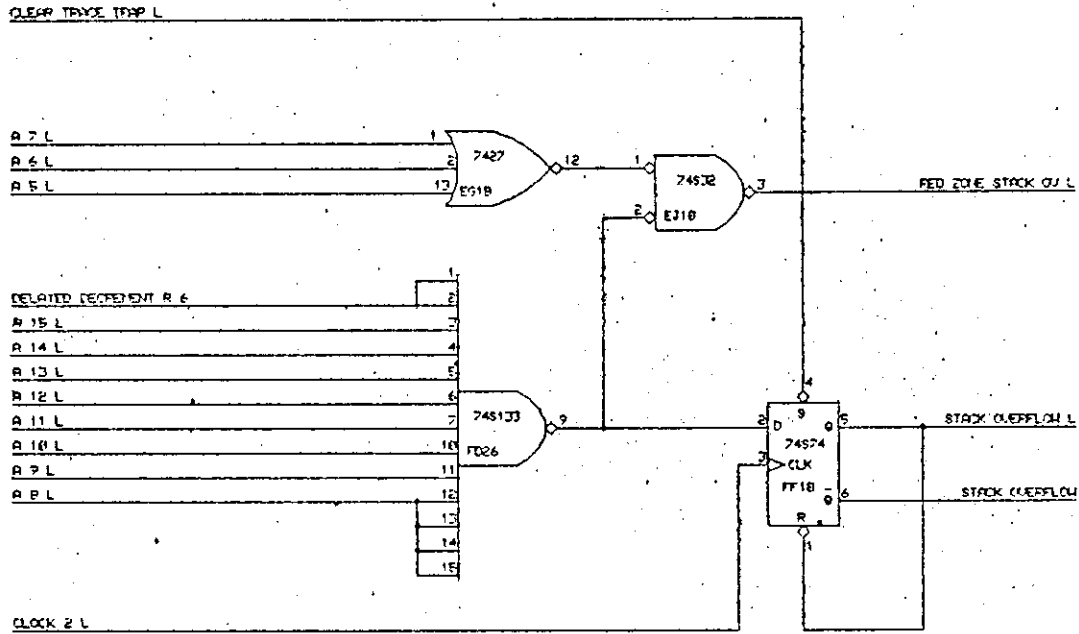
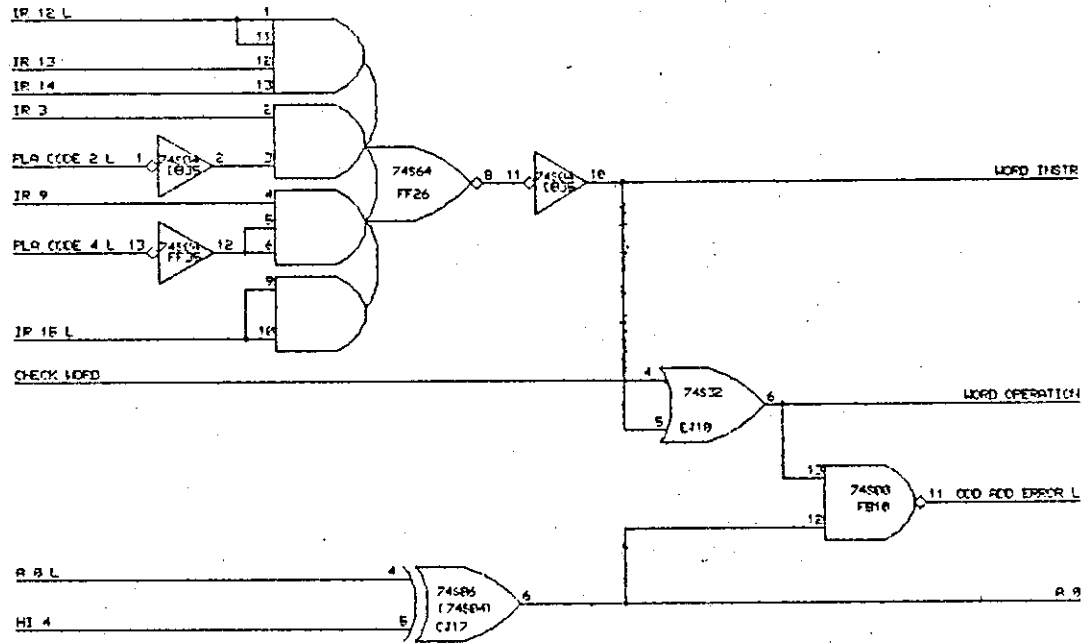
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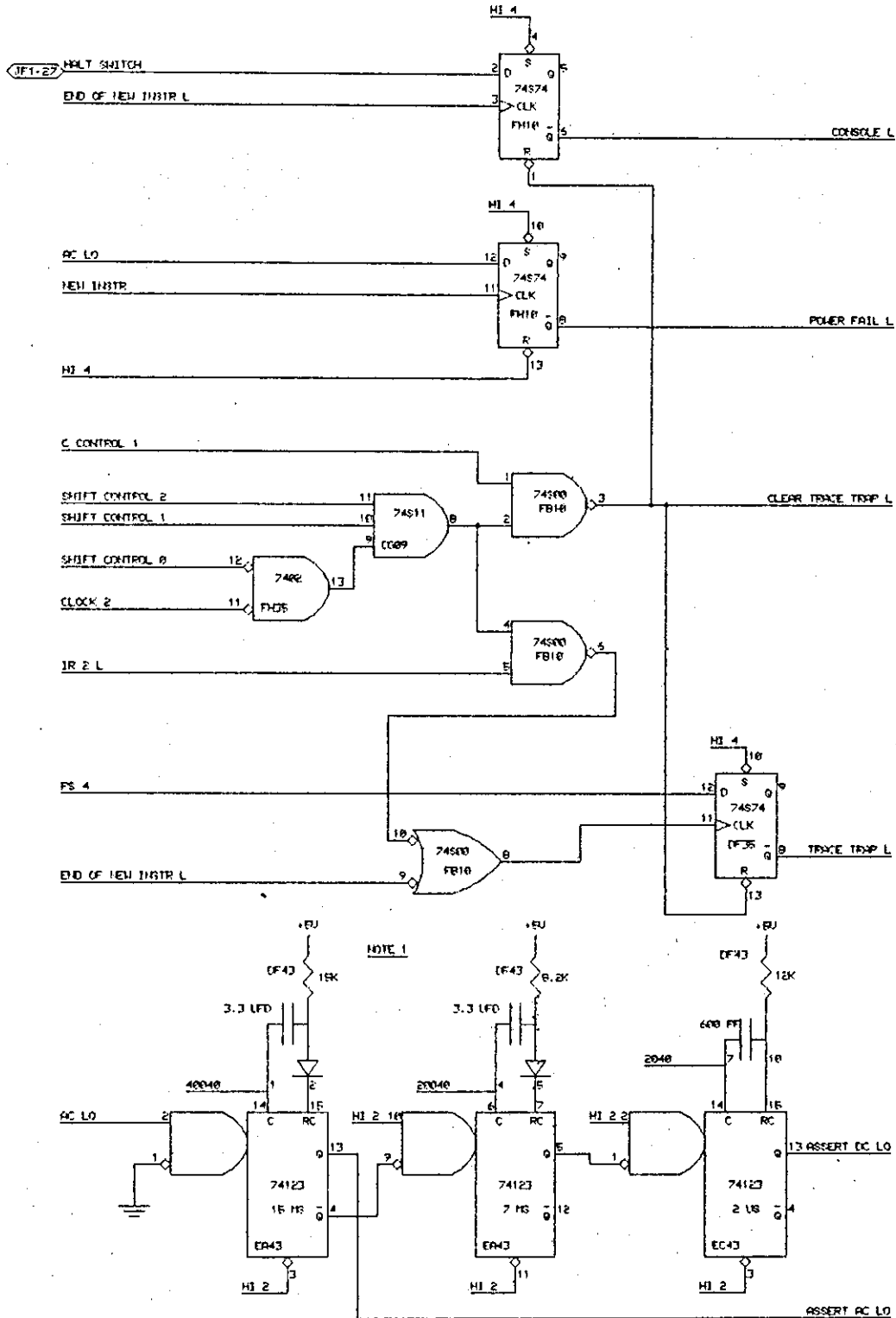
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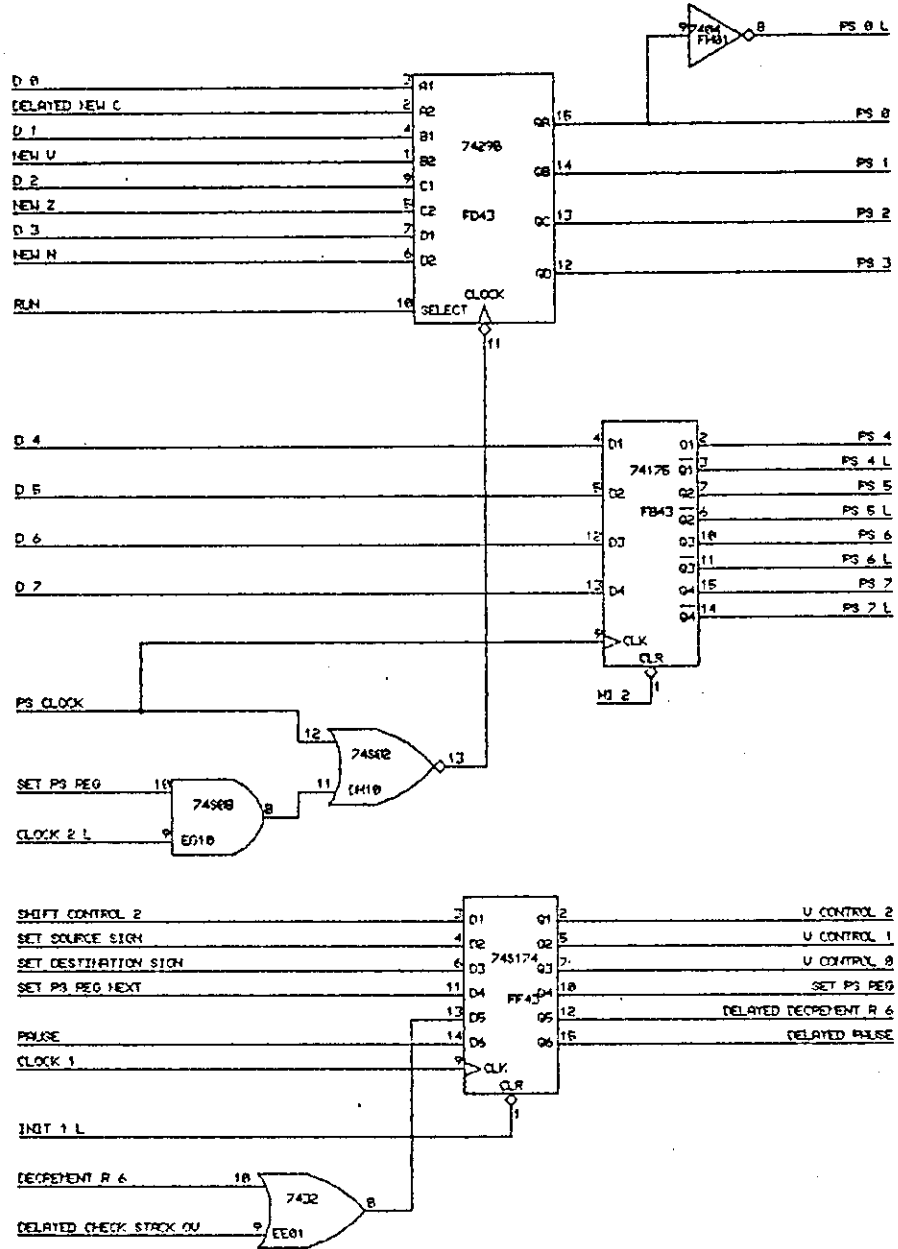
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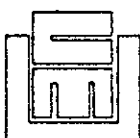


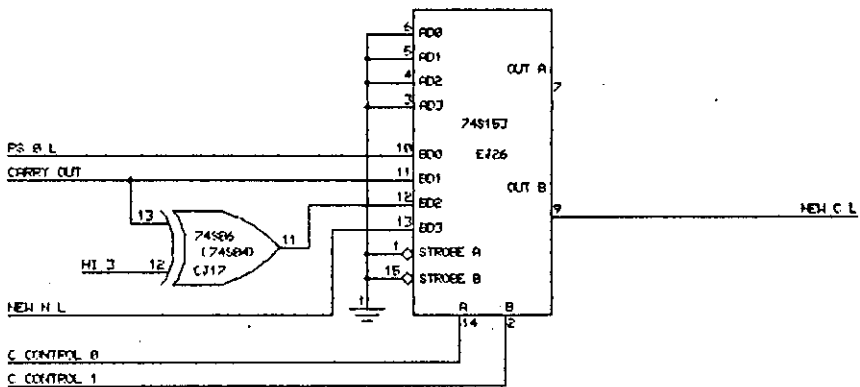
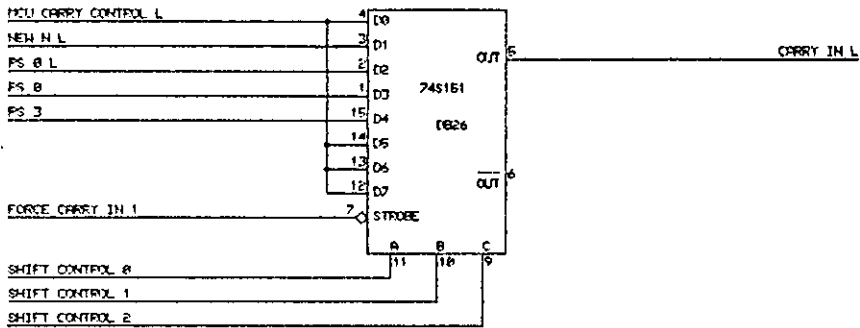
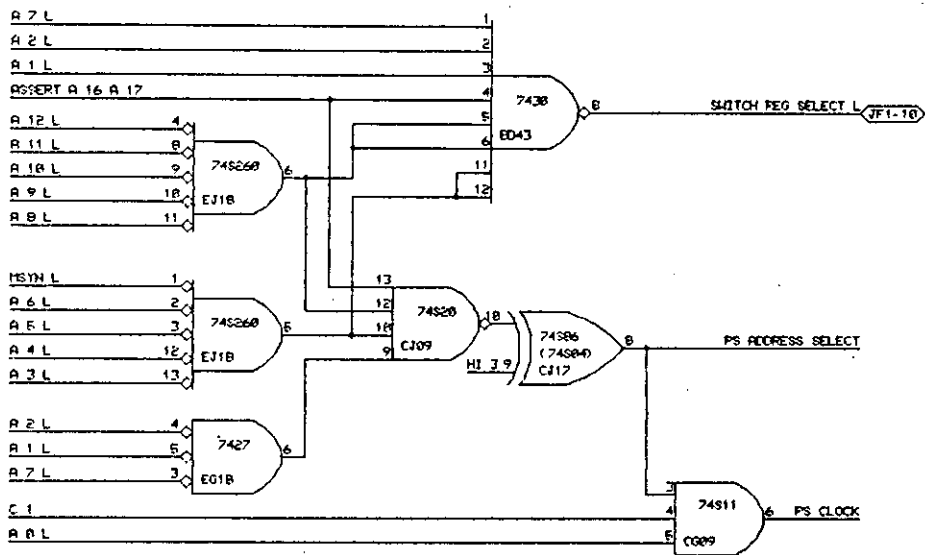
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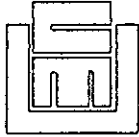
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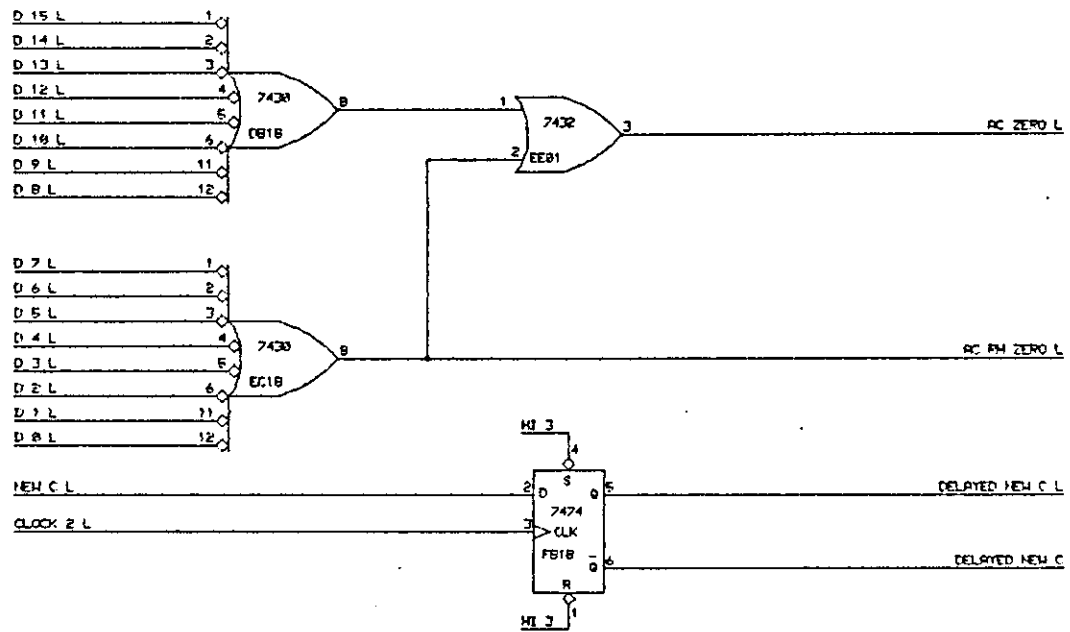
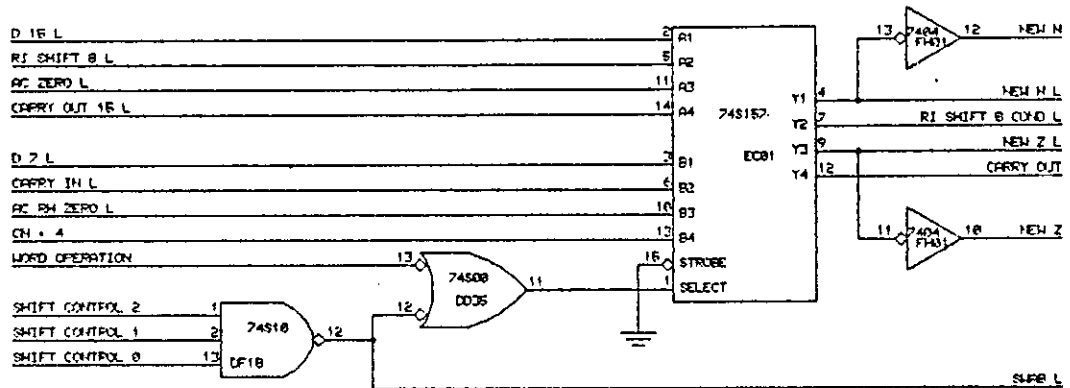
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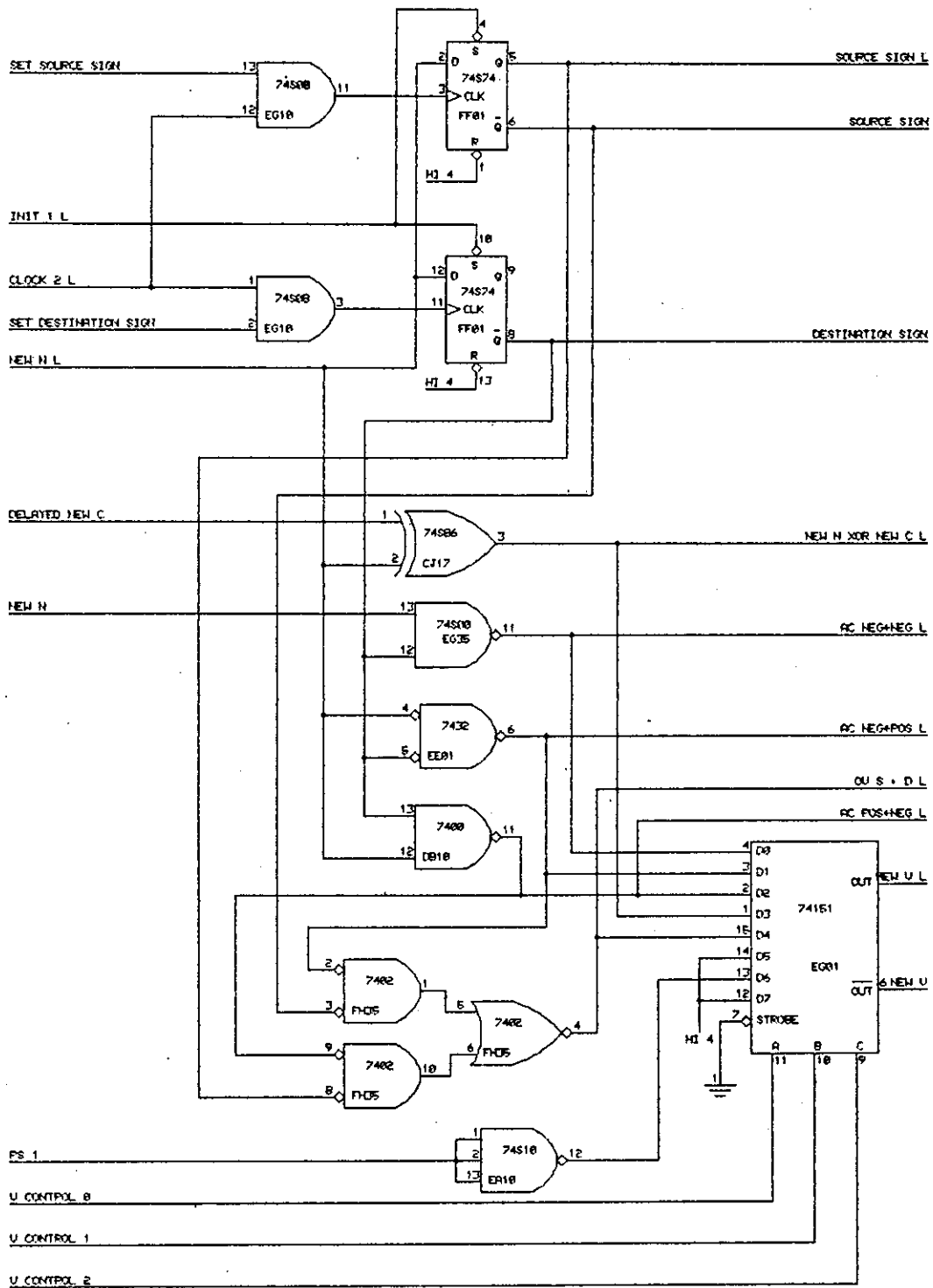
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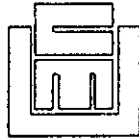


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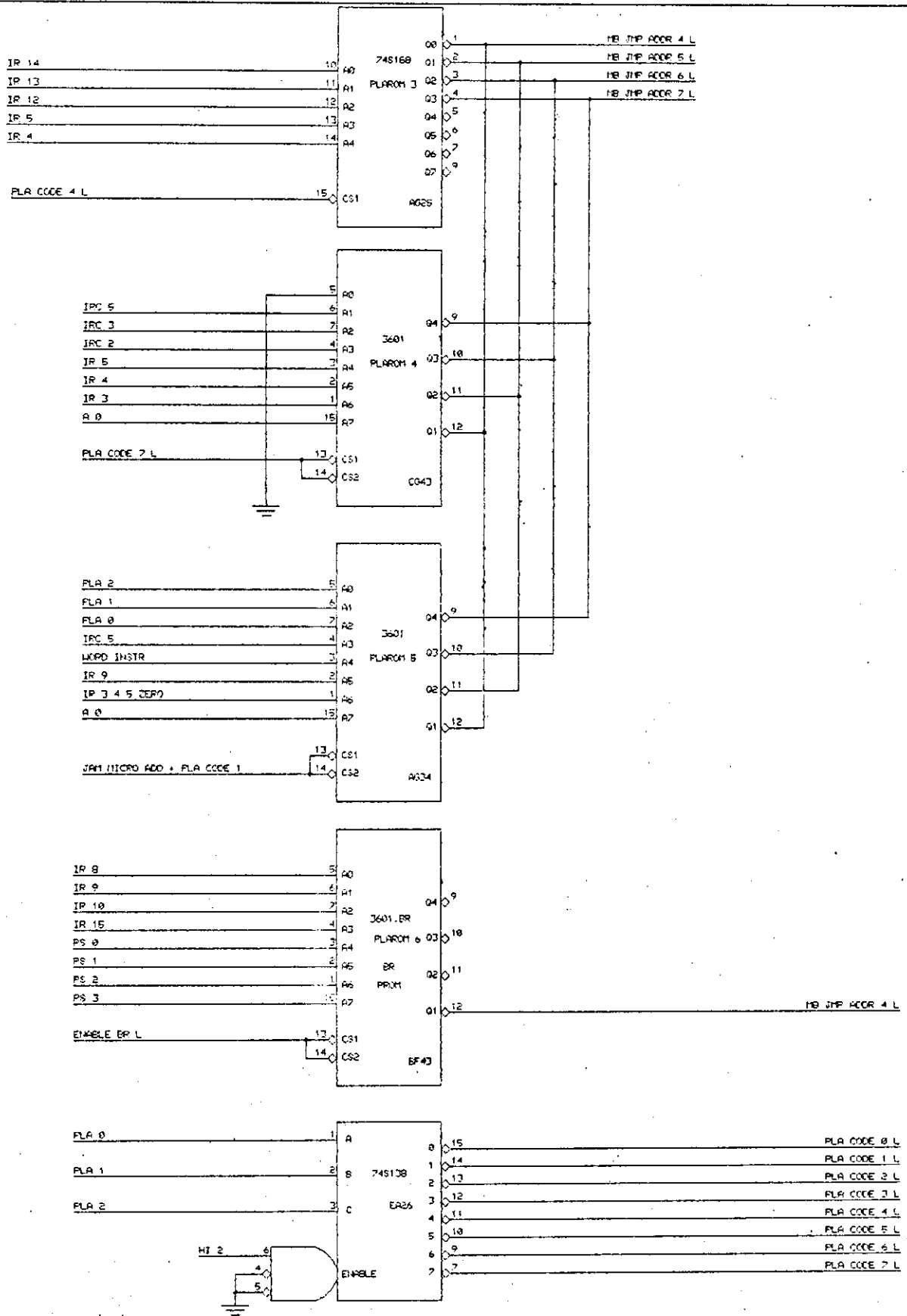


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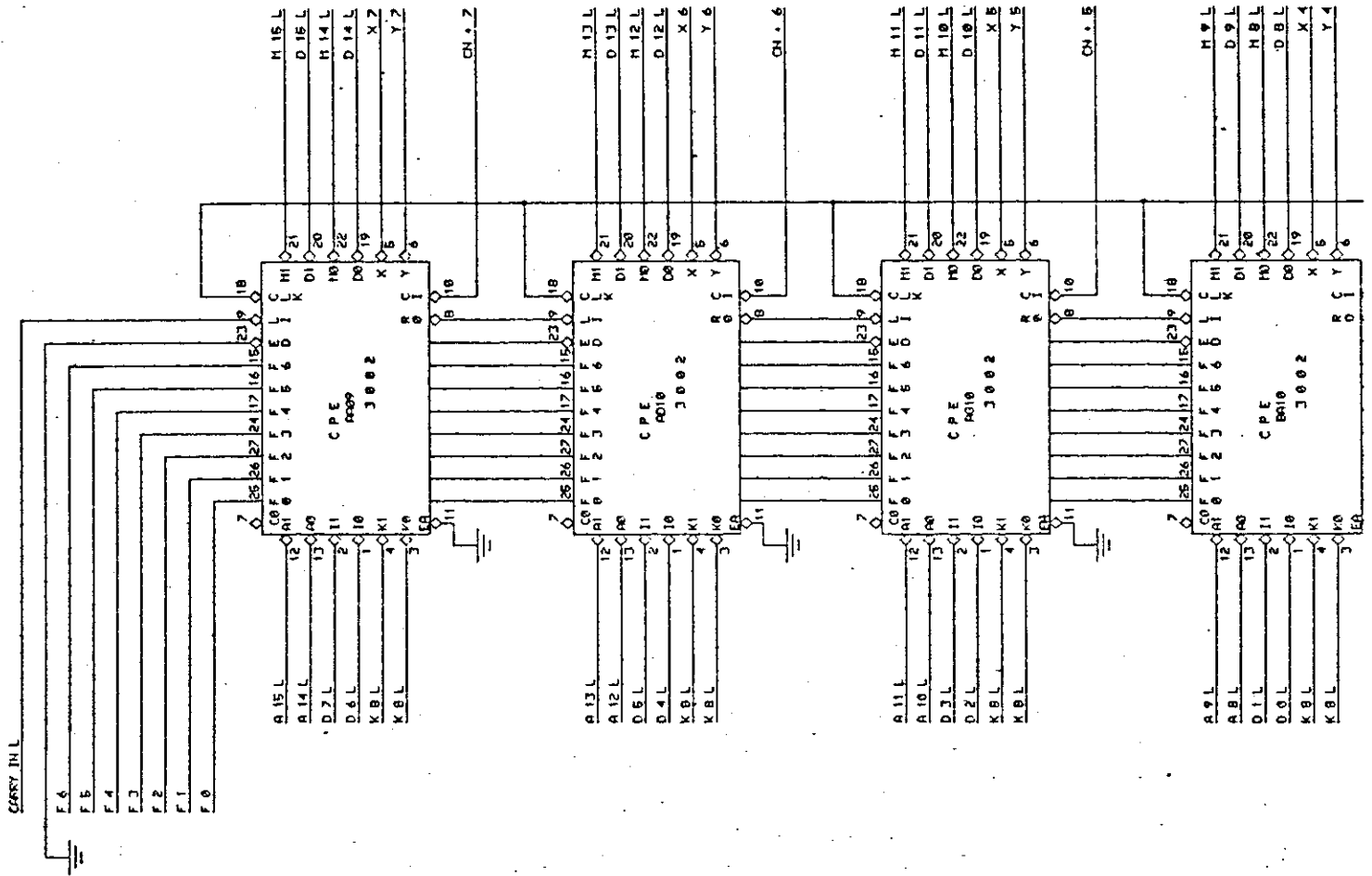


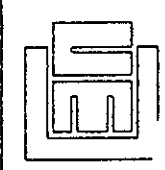
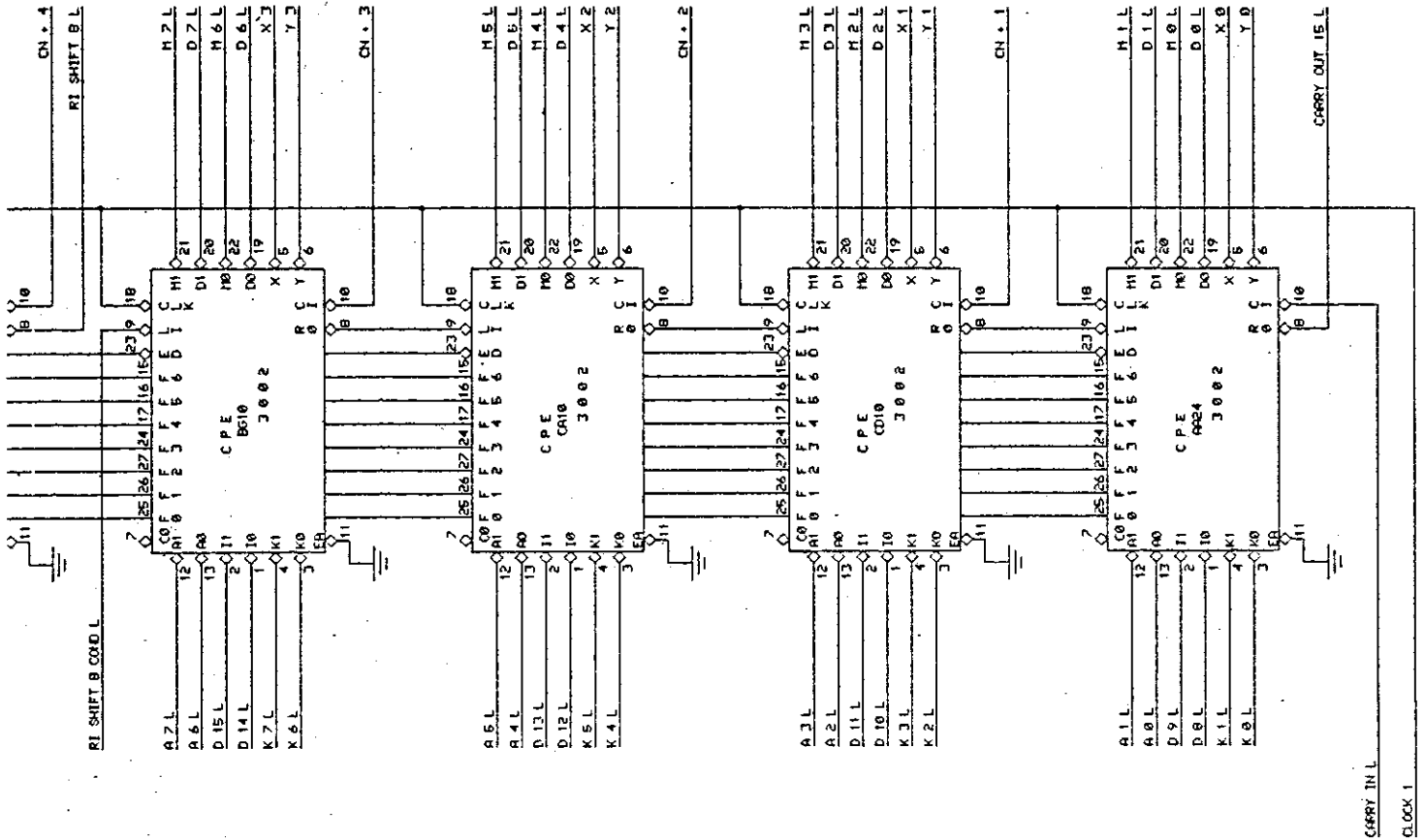
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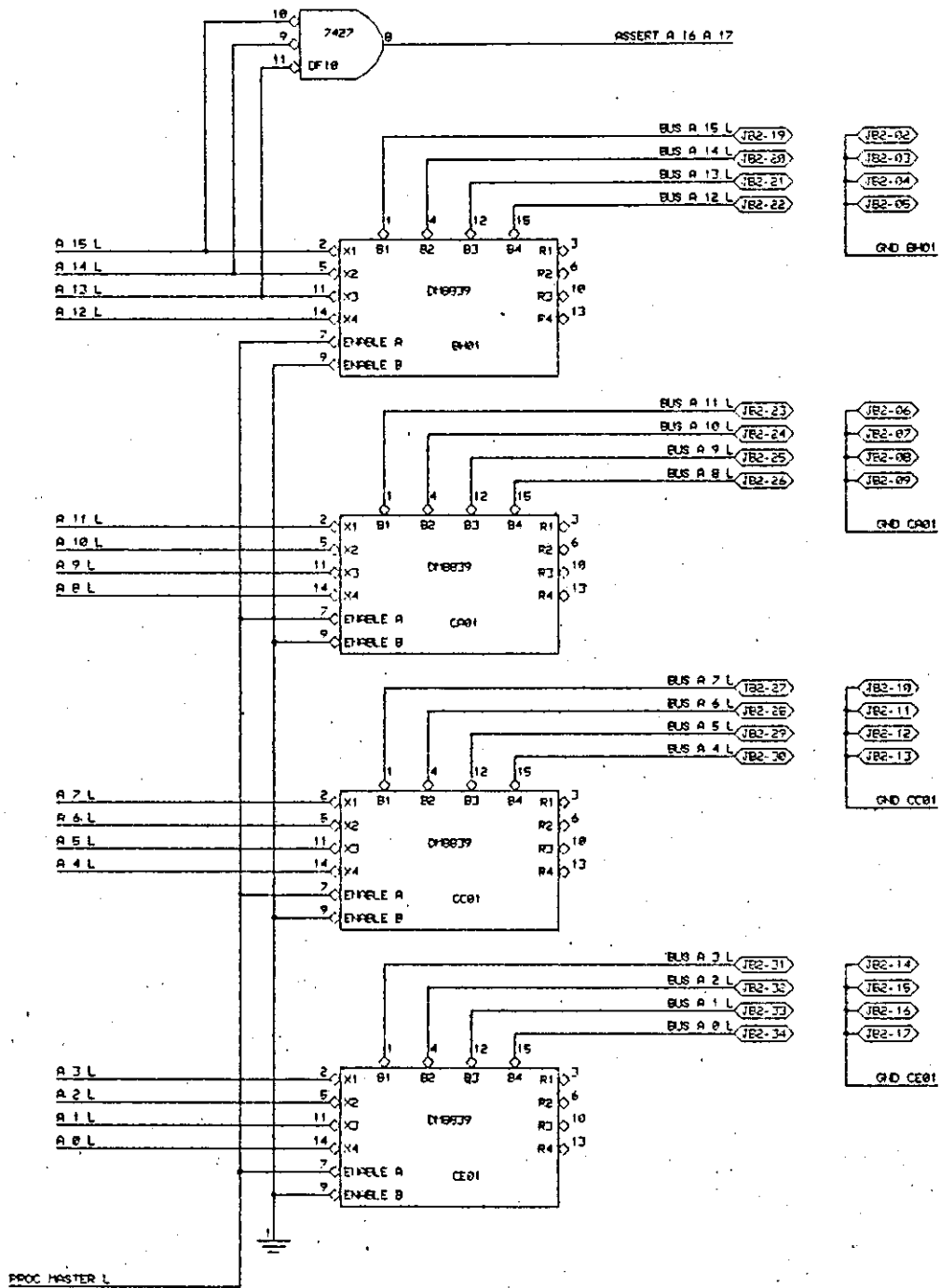


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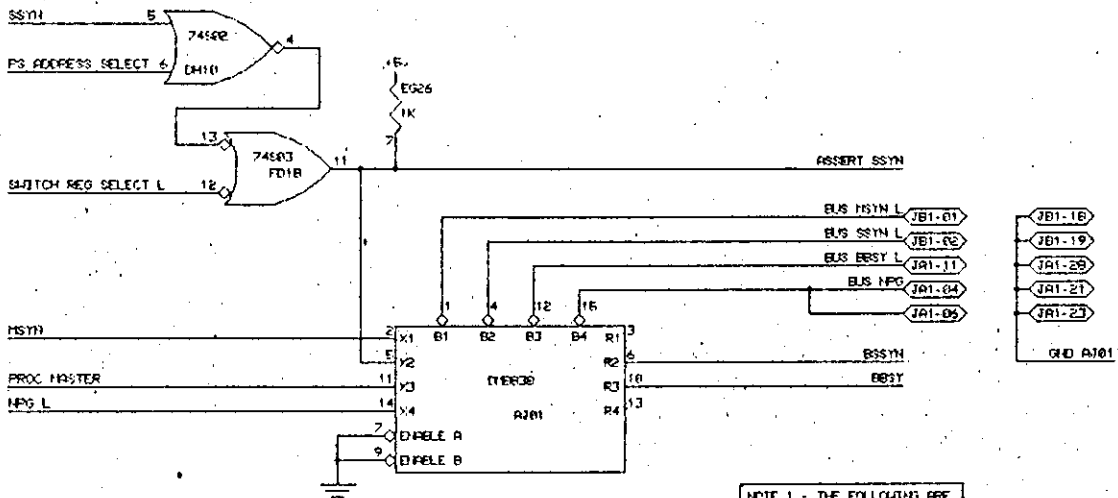




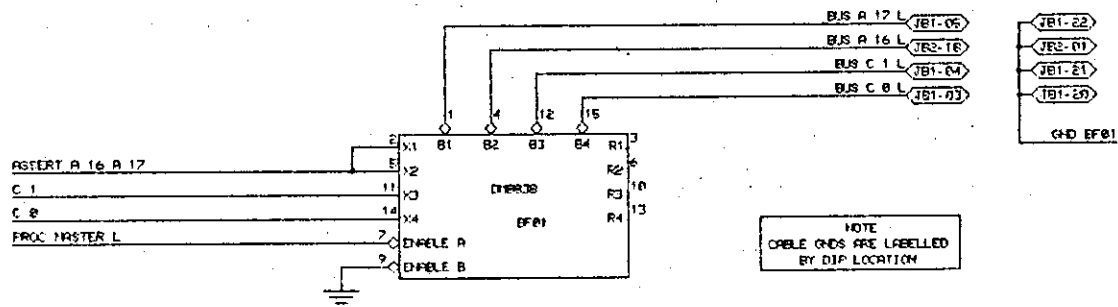
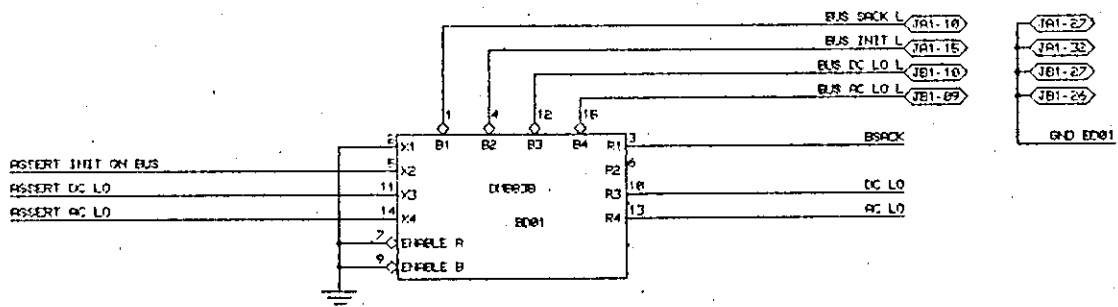
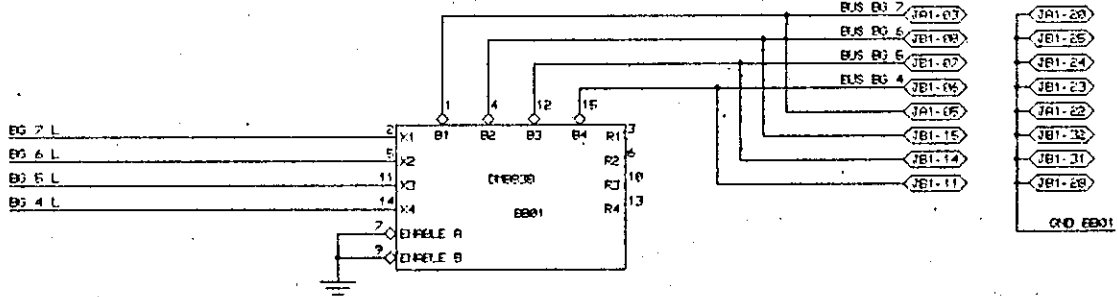
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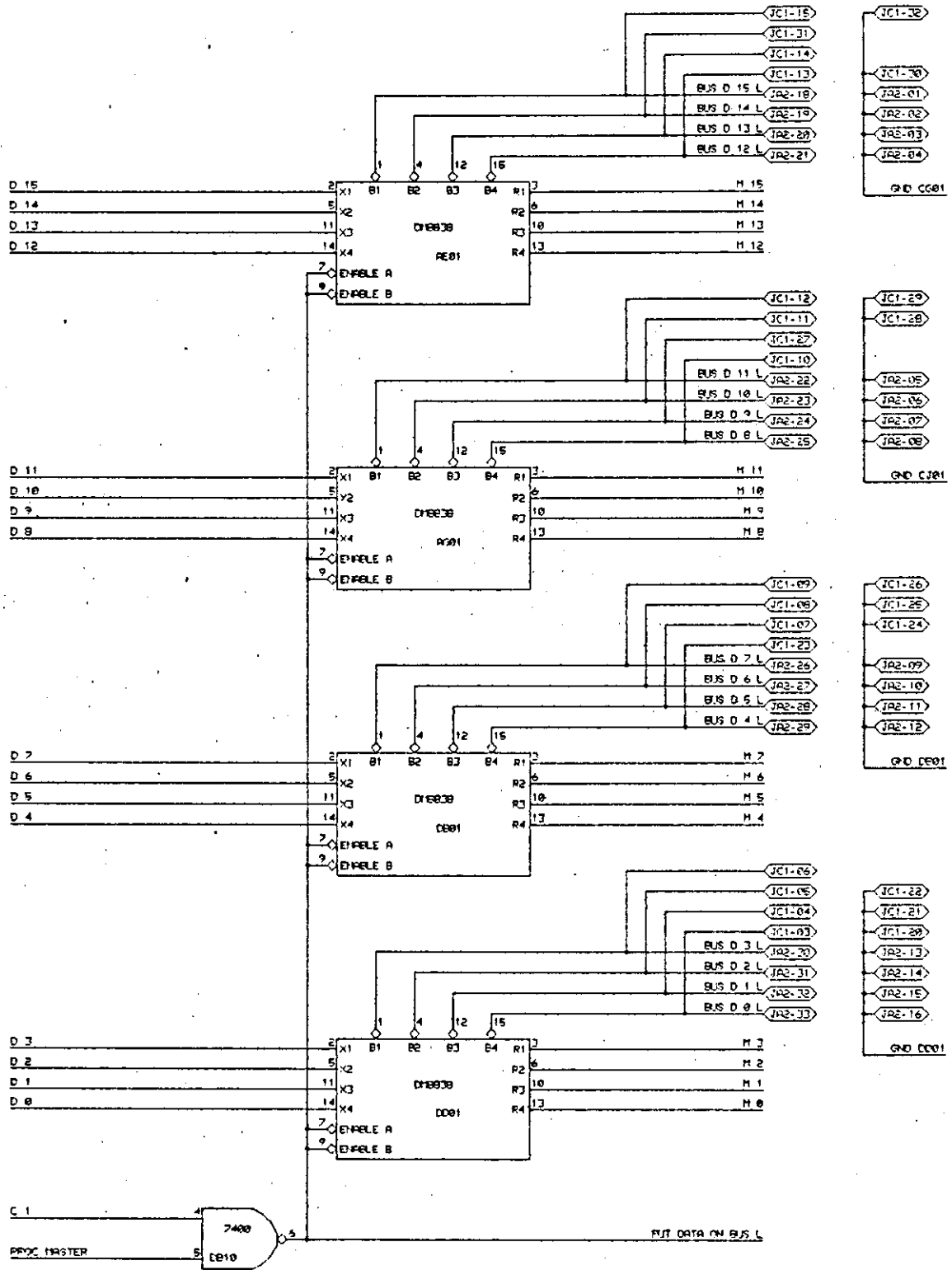


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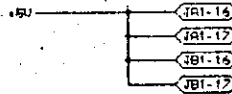
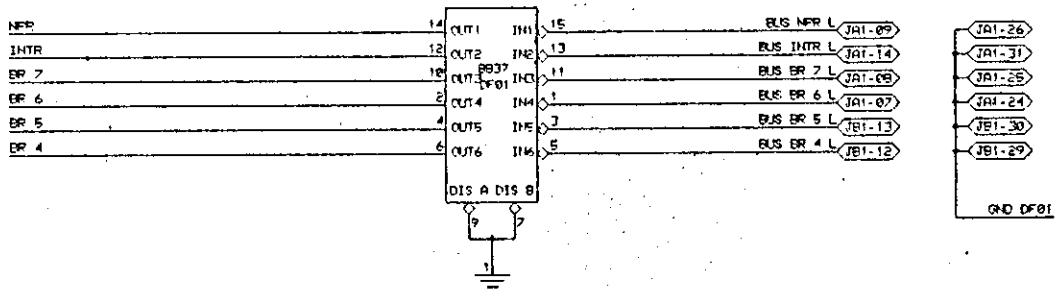
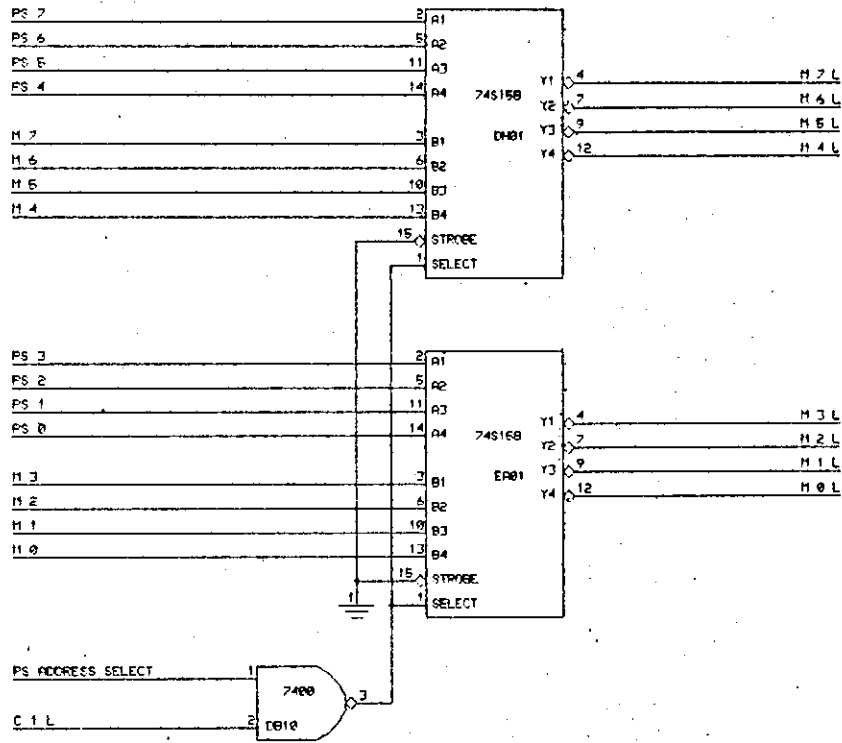


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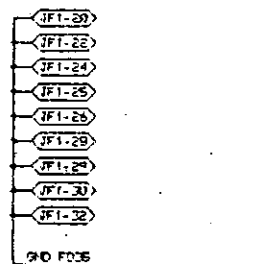
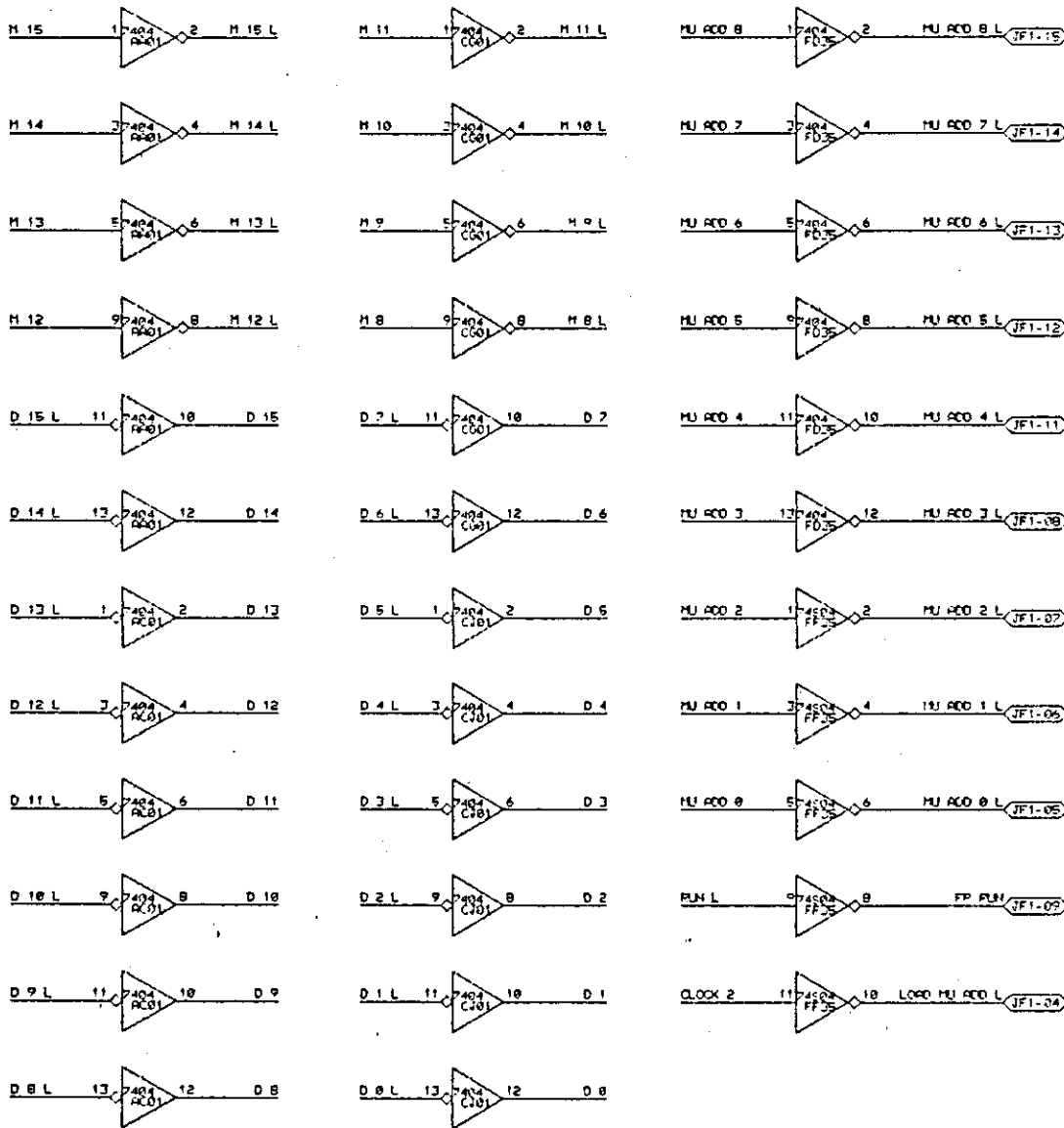


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PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR			
DESIGN BY:	SHERWOOD	CHECKED BY:	
DRAWING FILE:	UNIBUS[N210TM05]	DRAWING NUMBER:	
CARRIEGIE-MELLON UNIVERSITY		PAGE	OF
		DATE:	11-JUN-75 01:59
		PITTSBURGH, PENNSYLVANIA 15213	

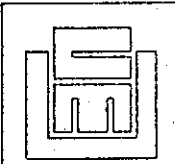
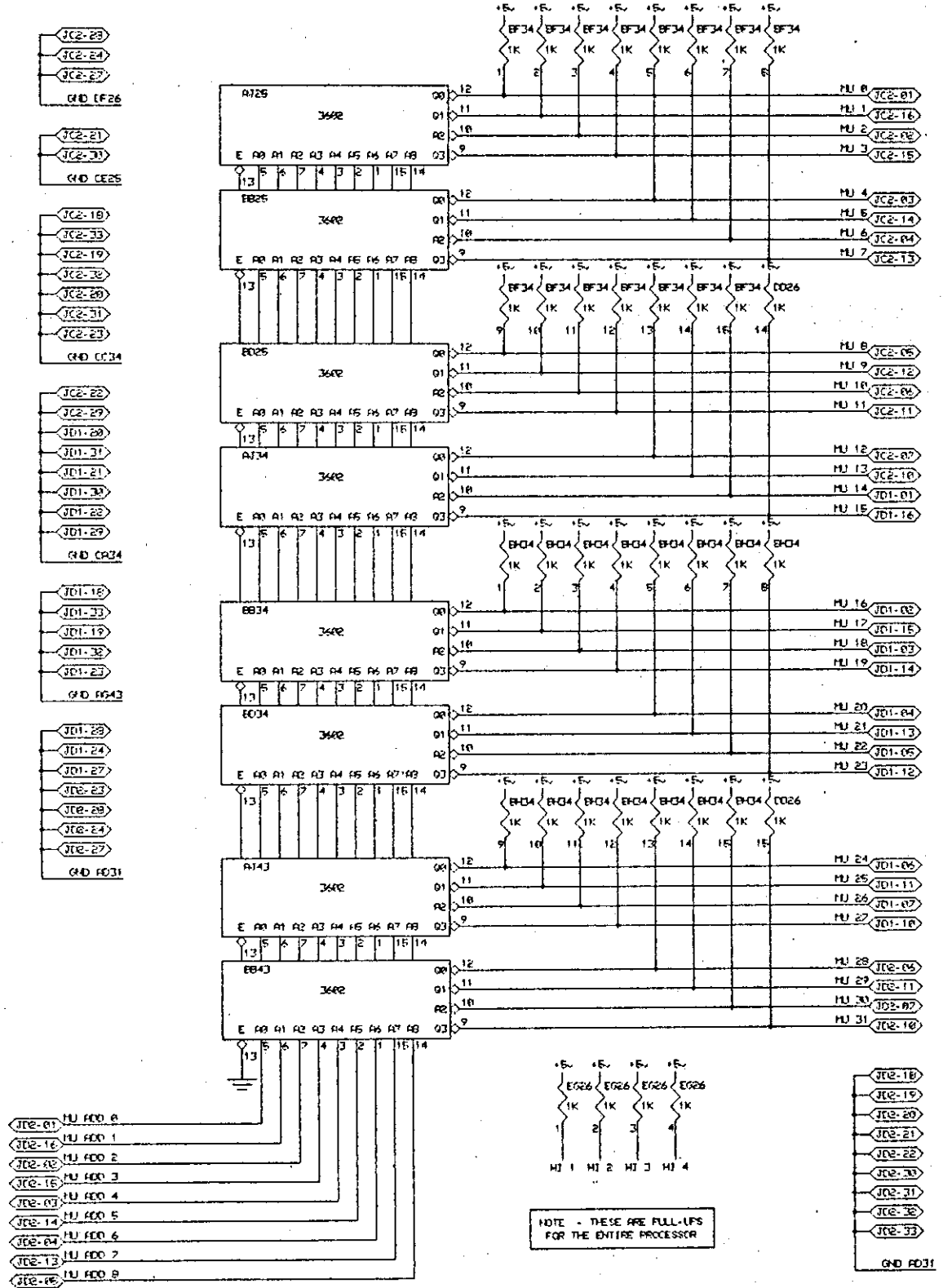


POWER FOR BUS TERMINATOR

	COMPUTER SCIENCE ENGINEERING LAB		
	TITLE: UNIBUS DATA INTERFACE		
	PROJECT: FDP-11, USING THE INTEL 3000 MICROPROCESSOR		
	DRAWN BY: SHERWOOD	CHECKED BY:	PAGE _____ OF _____
	DRAWING FILE: UNIMUX[N210TM05]	DRAWING NUMBER:	DATE: 02-JUN-75 18:06
CARRIEGIE-MELLON UNIVERSITY PITTSBURGH, PENNSYLVANIA 15213			

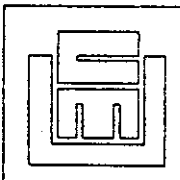
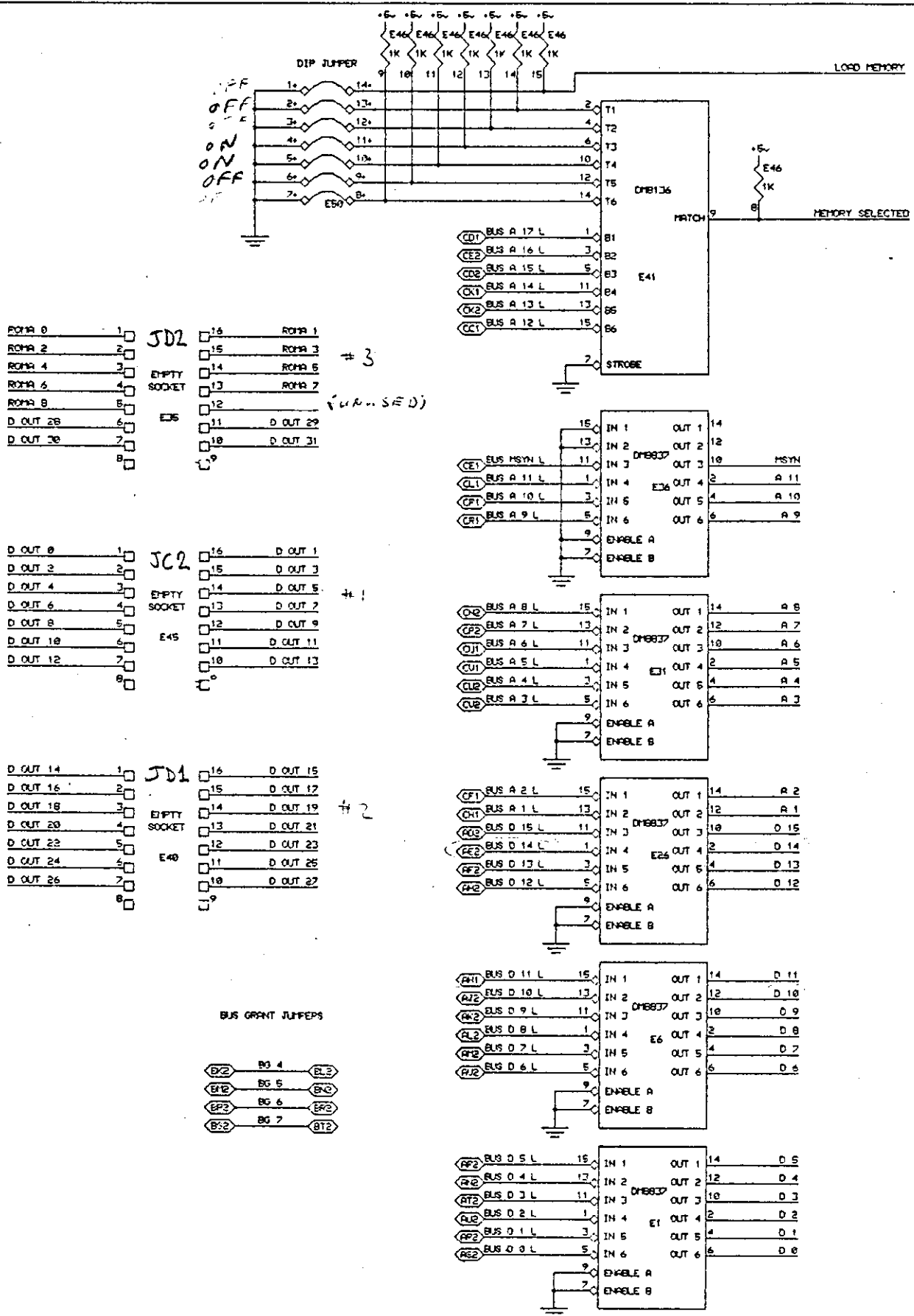


	COMPUTER SCIENCE ENGINEERING LAB	
	TITLE: INVERTERS FOR UNIBUS INTERFACE	
	PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR	
	DRAWN BY: SHERWOOD	CHECKED BY:
DRAWING FILE: UNINU[N210TMO5]	DRAWING NUMBER:	PAGE OF
CARNEGIE-MELLON UNIVERSITY		DATE: 12-JUN-75 03:13 PITTSBURGH, PENNSYLVANIA 15213



COMPUTER SCIENCE ENGINEERING LAB

TITLE: PROM CONTROL STORE	
PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR	
DESIGNED BY: SHERWOOD	CHECKED BY:
DATE: []	DATE: []
PAGE OF	
DATE: 30-MAY-75 08:02	
PITTSBURGH, PENNSYLVANIA 15261	



COMPUTER SCIENCE ENGINEERING LAB

TITLE: WRITEABLE CONTROL STORE - BUS INTERFACE

PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR

DESIGN BY: SHERWOOD

CHECKED BY:

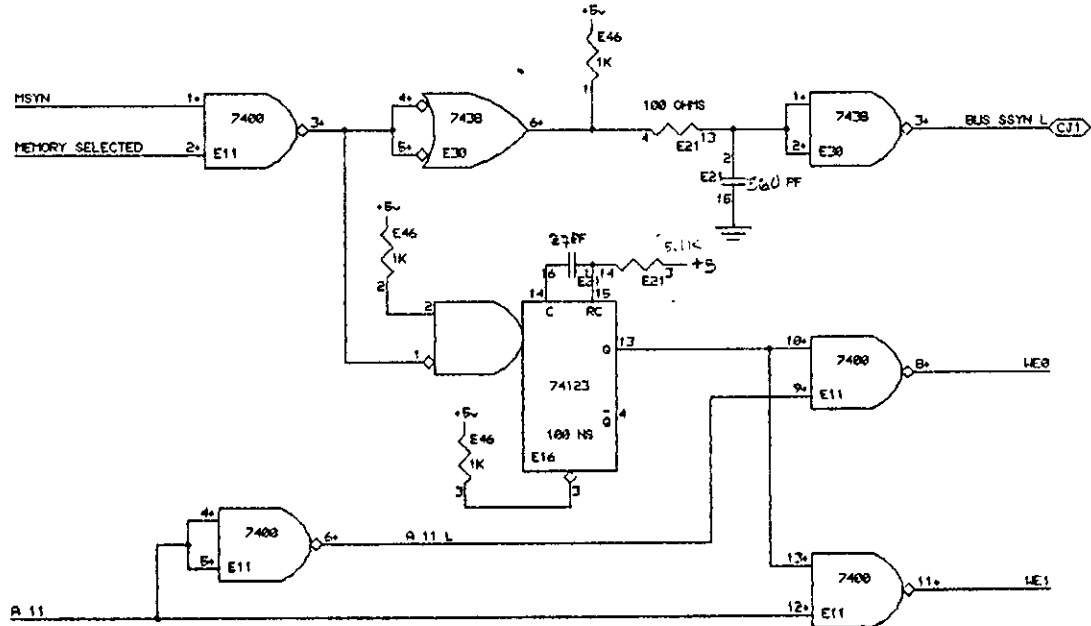
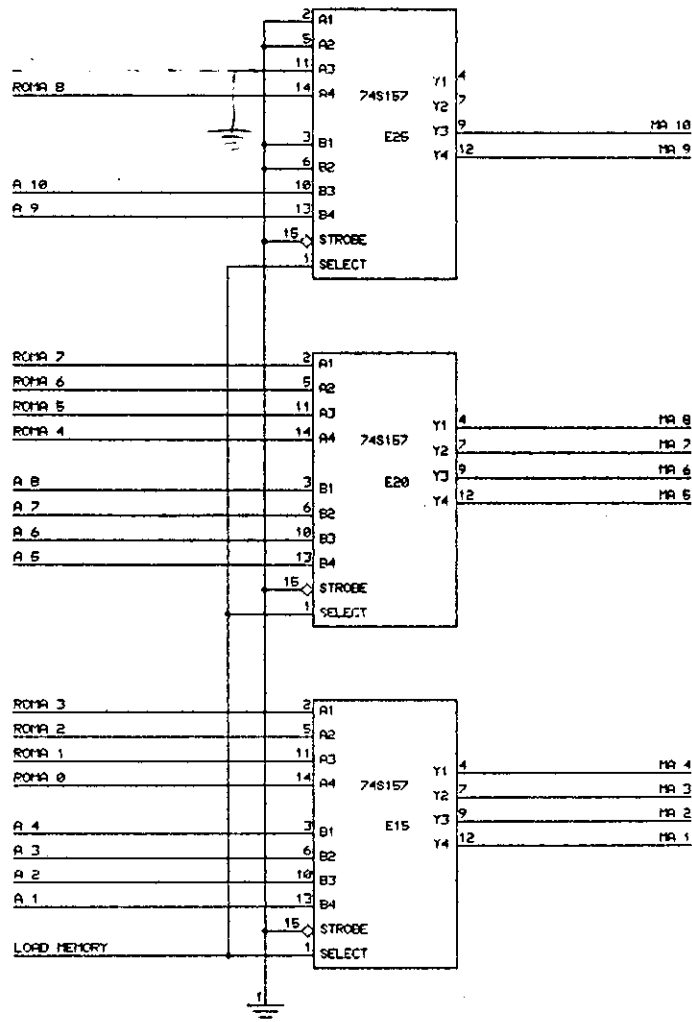
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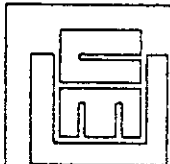
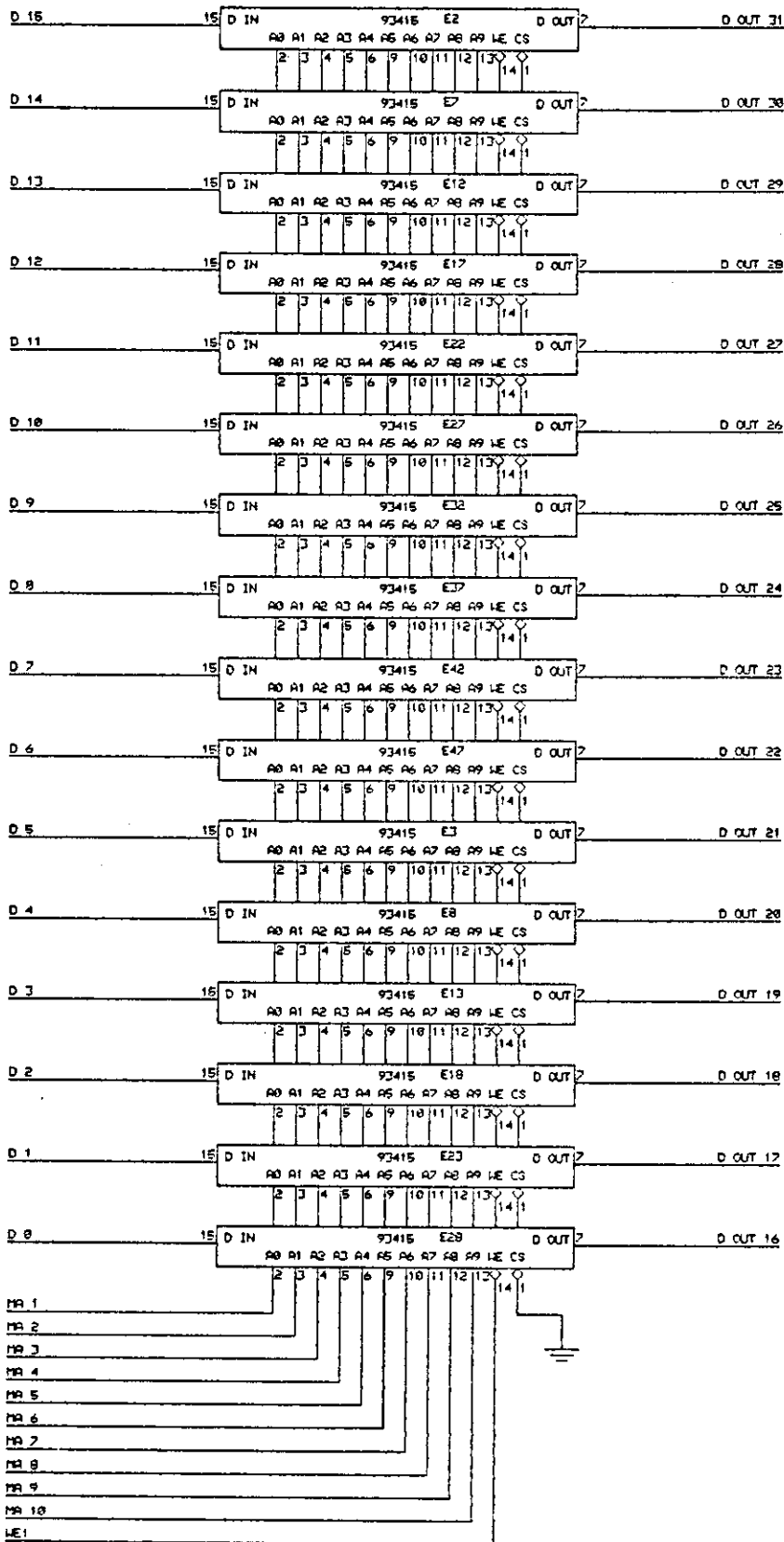
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DATE: 15-MAR-75 04:41

PITTSBURGH, PENNSYLVANIA 15213

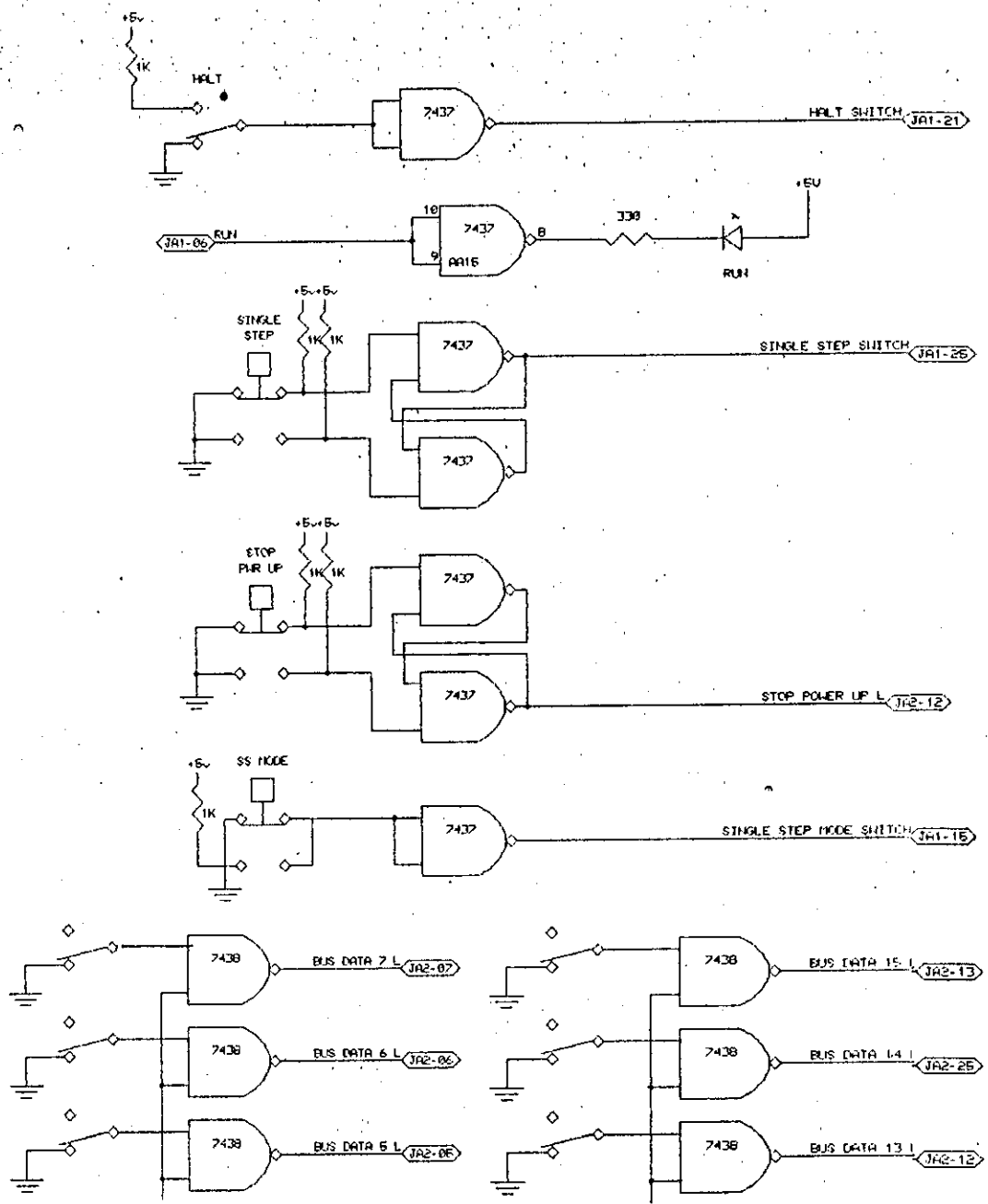


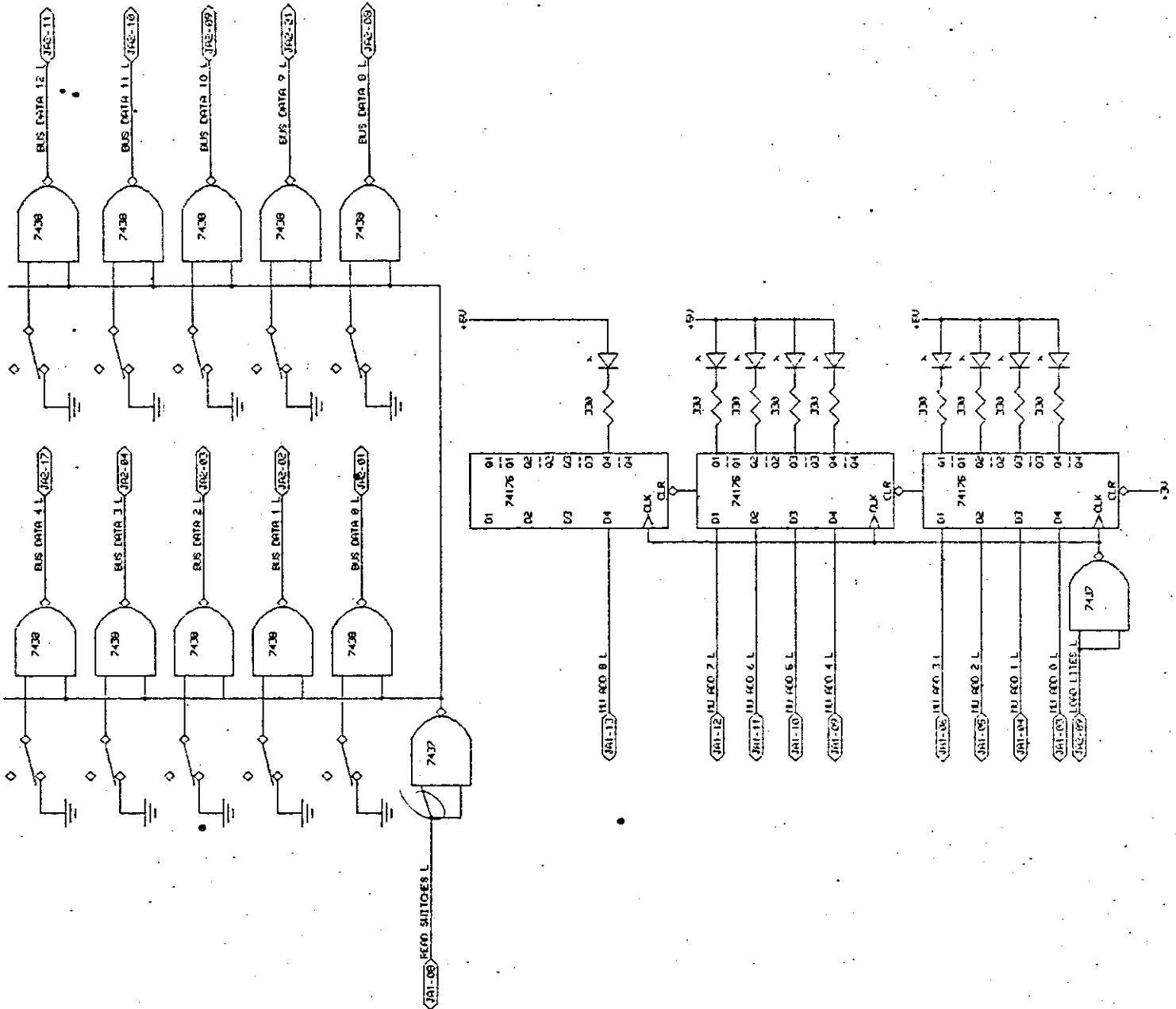
COMPUTER SCIENCE ENGINEERING LAB			
TITLE:			
PROJECT:			
DRAWN BY: SHERWOOD		CHECKED BY:	
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CARRIEGIE-MELLON UNIVERSITY		PAGE OF	
		DATE: 11-MAR-75 03:52	
		PITTSBURGH, PENNSYLVANIA 15213	

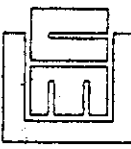


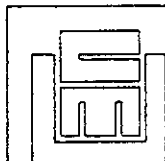
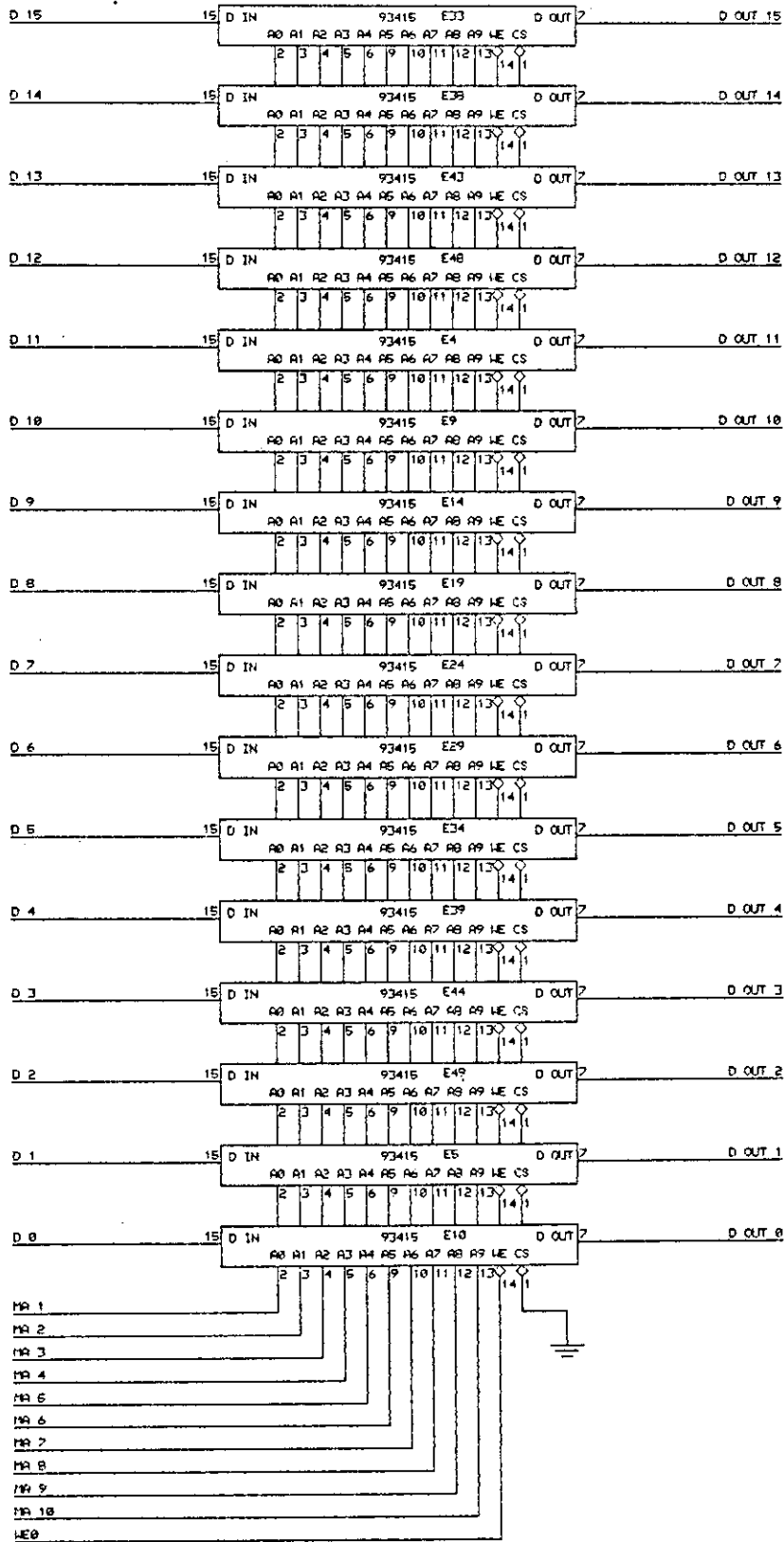
COMPUTER SCIENCE ENGINEERING LAB

TITLE: WRITEABLE CONTROL STORE	
PROJECT: PDP-11 USING THE INTEL 3000 MICROPROCESSOR	
DRAWN BY: SHERWOOD	CHECKED BY:
DRAWING FILE: STORE1[N210WS03]	DRAWING NUMBER:
PAGE _____ OF _____	
DATE: 10-MAR-75 22:24	
PITTSBURGH, PENNSYLVANIA 15213	





			COMPUTER SCIENCE ENGINEERING LAB		
TITLE: FRONT PANEL					
PROJECT:					
DRAWN BY:		CHECKED BY:			
DRAWING FILE: FPANEL [N210TM05]		DRAWING NUMBER:		PAGE: CF DATE: 19-JUN-75 03:58	
CARNEGIE-MELLON UNIVERSITY			PITTSBURGH, PENNSYLVANIA 15213		



COMPUTER SCIENCE ENGINEERING LAB

TITLE: WRITEABLE CONTROL STORE
 PROJECT: FDP-11 USING THE INTEL 3000 MICROPROCESSOR

DRAWN BY: SHERWOOD

CHECKED BY:

DRAWING FILE: STORE2[N210WS03]

DRAWING NUMBER:

PAGE: OF
 DATE: 10-MAR-75 22:29

ASSEMBLY OF MICRO.DAT ON 6-Jan-76 AT 10:48

ADDRESS	JMCD	OPCD	CYCD	PLA	KURG	MULTF
0000000	0011111	1111	122	2	22	22222333
1234567	8901234	5678	901	2	34	56789012

```

-----
;MICRO CODE TO MAKE A PDP-11/40 OUT OF THE INTEL 3000 ;
;MICRO PROCESSOR CHIPS.
;
;
;PROGRAMMING CONVENTIONS USED IN CODE:
;
; 1. ZERO IS KEPT IN R9 SO THAT TRAP ADDRESSES CAN EASILY BE
; PUT IN IT TO CALL THE TRAP SEQUENCE. THE TRAP SEQUENCE
; PUTS ZERO BACK IN R9 WHEN IT IS DONE.
;
; 2. THE Z BIT IS USED TO DETECT DOUBLE BUS ERRORS AND
; TO INDICATE THAT THE PROCESSOR IS IN CONSOLE MODE.
; IF IT IS SET AND A TRAP OCCURS, THE MICROPROCESSOR
; WILL JUMP TO THE CONSOLE CODE.
;
FIELD PLA 3,0:PLA1=1,PLA2=2,PLA3=3,PLA4=4,PLA5=5,PLA6=6,PLA7=7,&
NINST=0,INTSR=2,DECR=3,INCR=4,BUSWT=5,BREST=6,STKOV=7,&
WIF1=4,WIF3=2
FIELD KUB 1,1:KA1=0,KL1=0 ;NOTE: ALL K LINES ARE INVERTED.
FIELD RG12 2,3:RG1=2,RG2=0,RGD=1,KM0=3,KM1=2,KM10=1,KM11=0,&
KTY=2,SETS1=2,SETD1=1,&
SCLR1=1,STST1=1,SCOM1=1,STNC1=1,SDEC1=2,SNEG1=0,&
SASR1=3,SASL1=3,SROR1=3,SRDL1=3,SADC1=1,SSBC1=2,&
SNOV1=1,SBIT1=1,SBCS1=1,SDR1=1,SSXT1=1,SCMP1=0,&
SSUB1=0,SADD1=0,SSWB1=3,&
PSVS=1,PSVN=2
;
;MICRO WORD FOR I/O INSTRUCTIONS IS (8 BITS):
; EXTENDED INSTRUCTION,GET BUS(ASSERTED LOW),PAUSE,CHECK WORD,C(1:0),11B
;
FIELD MULTF 8,1000011B:EINS=11000011B,EGPMD=10110011B,EGWD1=10010011B,&
EPMD1=11110011B,EMD1=11010011B,PAUSE=1100011B,EGPWT=10100011B,&
EGD1=10000011B,EPHASE=11100011B,&
GPD1=110011B,GPMOP=110111B,GPMDO=111011B,GPMDB=111111B,&
GPD1P=100011B,GPD1P=100111B,GPD0=101011B,GPD0B=101111B,&
GWD1=010011B,GWD1P=010111B,GWD0=011011B,GWD0B=011111B,&
GD1=000011B,GD1P=000111B,GD0=001011B,GD0B=001111B,&
PMD1=1110011B,PMD1P=111011B,PMD0=1111011B,PMD0B=111111B,&
PD1=1100011B,PD1P=110011B,PD0=1101011B,PD0B=110111B,&
WD1=1010011B,WD1P=101011B,WDO=1011011B,WDOB=101111B,&
D1=1000011B,D1P=100011B,DO=1001011B,DOB=100111B,&
ED1=11000011B,ED1P=1100011B,EDO=11001011B,EDOB=1100111B,&
K0=1111101B,KR1=01B,KR2=101B,K1=1111101B,&
K2=11110101B,K4=1110101B,K7=11100001B,&
K10=1101101B,K14=1100101B,K17=11000001B,K20=1011101B,&
K21=10111001B,K24=10101101B,&
K30=10011101B,K34=1000101B,K35=10001001B,&
K40=0111101B,K57=01000001B,&
K60=111101B,K66=00100101B,K70=11101B,K71=00011001B,&
K77=01B,KCR=11001001B,KLF=11010101B,KRB=101B,&
KRM=01B,KZERO=0011101B,KSLSH=01000001B,&
KTK5=111101B,KTKB=110101B,KTP5=101101B,KTPB=100101B,&
SETS2=2,SETD2=2,&
SCLR2=01101110B,STST2=01101110B,SCOM2=10101110B,&
STNC2=00000110B,SDEC2=00000110B,SNEG2=10000110B,&
SASR2=01001110B,SASL2=11000110B,SROR2=01010110B,&
SRDL2=11010110B,SADC2=01010110B,SSBC2=10011110B,&
SNOV2=00101110B,SBIT2=00101110B,SBCS2=00101110B,&
SDR2=00101110B,SSXT2=00100110B,SCMP2=10110110B,&
SSUB2=10110110B,SADD2=01101110B,SSWB2=10111110B,&
SETTT=00110010B,CLRTT=10110010B,SSWB3=00111010B,&
PSC5=01111110B,PSCN=00111110B,PSC1N=00010010B
;

```

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-----
;PUT RESULT OF LAST INSTRUCTION IN MEMORY ;
;AND FETCH NEXT INSTRUCTION.
;

```

4	WDESRI	SDR R0,1,KA1,RGZ,JMP FETCH	:4 R(N)=AC	/00072/	000000100 0101011 0100000 1111 000 0 00 01000011
6	WOSRB	SDR T,1,KM11,K77	:6 T=AC AND 377	/00074/	000000110 0011101 0101100 1111 000 1 00 00000001
470		JLR R0,RGZ	:726 AC=R(NZ)	/00075/	111010110 0010010 0000000 0011 000 1 00 01000011
294		JLR T,KL1,K0	:446 AC,T+T(AC AND 177400)	/00076/	100100110 0011000 0001100 0011 000 0 11 11111101
398		SDR R0,1,KA1,RGZ,JMP FETCH	:606 R(NZ)=AC	/00077/	110000110 0101011 0100000 1111 000 0 00 01000011
0	WDESH	NOP GPMDO,JMP FETCH	:0 N(NAR)=AC	/00079/	000000000 0101011 0001101 0011 000 1 11 00111011
1	DDAD	LHJ R9,K4,JMP GTRAP	:1 TRAP TO LOC 4	/00081/	000000001 0101010 0011001 0011 000 1 11 11101101

```

; ODD ADDRESSING ERROR.
;
3 WDEOB: LDI AC,1,KAI ;3 ODD BYTE, SWAP HALVES /00084/ 00000011 010010 010111 1111 000 0 11 0100011
2 WDESB: NOP GPDOB,JMP FETCH ;2 M(MAR)=AC, BYTE /00085/ 00000010 010101 0001101 0011 000 1 11 00101111
;
;
11 FETCH: LMI R7,EGDI ; MAR=R(7) /00088/ 00000101 010011 001011 0011 000 1 11 1000011
7 FFET: ADR R7,1,EINS ;7 R(7)=R(7)+1 /00089/ 00000011 001010 011011 1111 000 1 11 1100011
358 AMA T,EPWDI ;547 T=INSTRUCTION /00090/ 10110011 011110 0001010 0011 000 1 11 11110011
366 ADR R7,1,PLA1 ;556 WAIT FOR INSTRUCTION DECOD/00091/ 10110110 0010101 011011 1111 001 1 11 0100011
350 LMI R7,0 STZ,PLA7,JMP 350 ;536 DO INITIAL DECODE /00092/ 10101110 0010101 001011 0001 111 1 11 0100011
;
; ON INSTRUCTION BY USING THE
; MICRO INTERRUPT FEATURE.
;MAR=R7,Z=0
;
;-----;
;LOAD SOURCE OPERAND INTO T. FORMAT IS 5500
;INSTRUCTION CLASS 1
;-----;
;
;REGISTER MODE=0: R(N)
;
80 SOP0: ILR R0,RG1,PLAZ ;120 AC=R(N) /00104/ 00101000 0111100 0000000 0011 010 1 10 0100011
92 NOP PLA4,JPX 64 ;132 /00105/ 001011100 1111000 0001101 0011 100 1 11 0100011
;
;REGISTER MODE=1: (R(N))+
;
81 SOP1: LMI R0,RG1,EGDI,INCR ;121 MAR=R(N), R(N)=R(N)+CONDIN/00109/ 001010001 0111011 0010000 0011 100 1 10 1000011
91 ILR R0,1,RG1,PLAZ,JMP SRCMR ;R(N),AC=R(N)+1 /00110/ 001011011 0111101 0000000 1111 010 1 10 0100011
;
;REGISTER MODE=2: -(R(N))
;
82 SOP2: LMI R0,KAI,RG1 ;122 R(N)=R(N)-1 /00114/ 001010010 0011010 0010000 0011 000 0 10 0100011
418 LMI R0,KAI,PG1,EINS,DECR ;R(N)=R(N)-1+CONDDCCR /00115/ 110100010 0111101 0010000 0011 011 0 10 1100011
429 LMI R0,RG1,GDI,JMP SRCM1 ;MAR=R(N) /00116/ 110101101 0010100 0010000 0011 000 1 10 0000011
;
;REGISTER MODE=3: X(R(N))
;
83 SOP3: LMI R7,1,GWDI ;123 MAR=R(7), R(7)=R(7)+1, /00120/ 001010011 0111111 0010111 1111 000 1 11 00010011
95 ILR R7,1,WDI ;R(7)=R(7)+1 /00121/ 001011111 0010001 0000111 1111 000 1 11 01010011
287 ILR R0,RG1,WDI ;AC=R(N1) /00122/ 100011111 0111110 0000000 0011 000 1 10 01010011
286 AMA AC,KAI,PWDI ;AC=AC+M(MAR) /00123/ 100011110 0010100 0001011 0011 000 0 11 01110011
334 LMI AC,GDI ;MAR=AC /00124/ 101001110 0111101 0011101 0011 000 1 11 00000011
333 SRCM1: NOP PLAZ,DI ;ALLOWS ADDR LINES TO SETTLE /00125/ 101001101 0000101 0001101 0011 010 1 11 01000011
93 SRCMR: LTM AC,KAI,POI,PLA4,JPX 64 ;135 AC=M(MAR) /00126/ 001011101 1111000 1011011 0011 100 0 11 01100011
;
;
65 SIPB: SDR T,1,KAI,PLA7,SETS1,SETS2,JPX 64 /00120/ 001000001 1111000 0101100 1111 111 0 10 00000010
;
;101 DO CALCULATE SECOND OPERAND
;PUT SOURCE OPERAND INTO T AND
;SET SOURCE SIGN BIT.
;
;INDIRECT BIT SET
;
66 SDEF: LMI AC,GDI ;102 MAR=AC /00135/ 001000010 0010000 0011101 0011 000 1 11 00000011
258 NOP DI ;NEEDED TO DO ADDRESSING /00136/ 100000010 0111110 0001101 0011 000 1 11 01000011
270 LTM AC,KAI,PLA3,POI /00137/ 100001110 0000101 1011011 0011 011 0 11 01100011
94 NOP PLA4,JPX 64 ;T=M(MAR) /00138/ 001011110 1111000 0001101 0011 100 1 11 01000011
;
;
67 SOBTT: LDI AC,1,KAI,PLA4,JMP SIRB ;103 AC=AC SWAPPED /00140/ 001000011 0110001 0101111 1111 100 0 11 01000011
;
;-----;
;LOAD DESTINATION'S ORIGINAL VALUE INTO AC IF USED
;IN INSTRUCTION.
;INSTRUCTION CLASS 2
;-----;
;
;REGISTER MODE=0: R(N)
;
68 DUSE0: ILR R0,RG2,JPX DU1PB ;104 AC=R(N2) /00150/ 001000100 1111011 0000000 0011 000 1 00 01000011
;
;REGISTER MODE=1: (R(N))+
;
69 DUSE1: LMI R0,1,PG2,GDIP ;105 MAR=R(N), R(N)=R(N)+1, /00154/ 001000101 0011001 0010000 1111 000 1 00 0000011
405 ILR R0,PG2,EDIP,INCR ;R(N),AC=R(N)+CONDINCR /00155/ 110010101 0110110 0000000 0011 100 1 00 11000111
406 NOP PLA7,DIP,JMP DESMR /00156/ 110010110 0000111 0001101 0011 111 1 11 0100011
;
;REGISTER MODE=2: -(R(N))
;
70 DUSE2: LMI R0,KAI,RG2 ;106 R(N)=R(N)-1 /00160/ 001000110 0011011 0010000 0011 000 0 00 01000011
438 LMI R0,KAI,RG2,EINS,DECR ;866 R(N)=R(N)-1+CONDDCCR /00161/ 110110110 0010100 0010000 0011 011 0 00 11000011
326 LMI R0,RG2,GDIP,JMP DESM1 ;S26 MAR=R(N) /00162/ 101000110 0011010 0010000 0011 000 1 00 0000011
;
;REGISTER MODE=3: X(R(N))
;
71 DUSE3: LMI R7,1,GWDI ;107 MAR=R(7), R(7)=R(7)+1 /00166/ 001000111 0010101 0010111 1111 000 1 11 00010011
343 ILR R7,1,WDI ;R(7)=R(7)+1 /00167/ 101010111 0110101 0000111 1111 000 1 11 01010011
341 ILR R0,RG2,WDI ;AC=R(N2) /00168/ 101010101 0010110 0000000 0011 000 1 00 01010011
357 AMA AC,KAI,PWDI ;AC=AC+M(MAR) /00169/ 101100101 0110110 0001011 0011 000 0 11 01110011

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358      LMI AC,GOIP          ;546 MAR=AC          /00170/  101100110 0011010 0011101 0011 000 1 11 00000111
422 DESM:  NOP PLA7,DIP      ;ALLOWS ADDR LINES TO SETTLE /00171/  110100110 0000111 0001101 0011 111 1 11 01000111
110 DESM:  LTM AC,KAI,WIF13,PDIP,JPX DU1RB ;156 AC=M(MAR) /00172/  001110110 1111011 1011011 0011 010 0 11 01100111
;
112 DU1RB:  NOP SETD1,SETD2,PLAS ;160 JUMP TO INSTRUCTIONS ACC. /00175/  001110000 0101101 0001101 0011 101 1 01 00000010
13  DU1B1:  NOP JPX ADC       ;15          /00176/  000001101 1111001 0001101 0011 000 1 11 01000011
;
;INDIRECT BIT SET
;
113 DUDEF:  NOP GDD          ;161 DIP MUST BE FOLLOWED BY A D/00180/  001110001 0011000 0001101 0011 000 1 11 00001011
385      NOP                  ;              /00181/  110000001 0111011 0001101 0011 000 1 11 01000011
395      NOP PDD            ;              /00182/  110001011 0000111 0001101 0011 000 1 11 01101011
123 DUDEF:  LMI AC,GOIP,PLA6 ;173 MAR=AC          /00183/  001111011 0111100 0011101 0011 110 1 11 00000111
124      LTM AC,KAI,PDIP,JPX DU1RB ;              /00184/  001111100 1111011 1011011 0011 000 0 11 01100111
;
114 DUOB:  LDI AC,1,KAI,PLAS,JMP DU1B1 ;162 DDD BYTE /00186/  001110010 0101101 0101111 1111 101 0 11 01000011
;
;-----;
;CALCULATE DESTINATION'S ADDRESS AND PUT IT IN MAR AND AC;
;INSTRUCTION CLASS 3
;-----;
;
;REGISTER MODE=0: R(N)
;
72  DA0:  ILR R0,RG2,JPX DU1RB ;110 AC=R(N)          /00195/  001001000 1111011 0000000 0011 000 1 00 01000011
;
;REGISTER MODE=1: (R(N))+
;
73  DA1:  ILR R0,RGZ          ;111 AC=R(N)          /00199/  001001001 0011100 0000000 0011 000 1 00 01000011
457      ADR R0,RGZ,EINS,INCR ;R(N)=R(N)+CONDINCR /00200/  111001001 0111111 0110000 0011 100 1 00 11000011
463      ADR R0,1,RGZ,PLA7    ;R(N)=R(N)+1        /00201/  111001111 0000111 0110000 1111 111 1 00 01000011
127 JDURB: LMI AC,JPX DU1RB ;177 MAR=AC          /00202/  001111111 1111011 0011101 0011 000 1 11 01000011
;
;REGISTER MODE=2: -(R(N))
;
74  DA2:  LMI R0,KAI,RGZ      ;112 R(N)=R(N)-1     /00206/  001001010 0000011 0010000 0011 000 0 00 01000011
58      LMI R0,KAI,RGZ,EINS,DECR ;R(N)=R(N)-1+CONDECR /00207/  000111010 0111111 0010000 0011 011 0 00 11000011
63      ILR R0,RG2,PLA7,JMP JDURB ;AC=R(N)           /00208/  000111111 0000111 0000000 0011 111 1 00 01000011
;
;REGISTER MODE=3: X(R(N))
;
75  DA3:  LMI R7,1,GWDI       ;113 MAR=R(7), R(7)=R(7)+1. /00212/  001001011 0000010 0010111 1111 000 1 11 00010011
43      ADR R7,1,WDI          ;R(7)=R(7)+1        /00213/  000101011 0111100 0101011 1111 000 1 11 01010011
44      ILR R0,RGZ,WDI        ;AC=R(INZ)          /00214/  000101100 0111111 0000000 0011 000 1 00 01010011
47      AMA AC,KAI,PLA7,PHDI,JMP JDURB ;AC=AC+M(MAR)      /00215/  000101111 0000111 0001011 0011 111 0 11 01110011
;
116 DA1RB:  NOP SETD1,SETD2,PLAS ;164          /00217/  001110100 0101001 0001101 0011 101 1 01 00000010
9  DA1B1:  NOP JPX SXT        ;JUMP TO INSTRUCTIONS SXT, ... /00218/  000001001 1111010 0001101 0011 000 1 11 01000011
;
;INDIRECT BIT SET
;
117 DADEF:  AMA AC,GPWDI      ;165          /00222/  001110101 0111110 0001011 0011 000 1 11 00110011
126 DADEF:  LMI AC,JMP DA1RB ;MAR=AC           /00223/  001111110 0110100 0011101 0011 000 1 11 01000011
;
;-----;
;LOAD SOURCE OPERAND INTO AC.  FORMAT IS SS ;
;INSTRUCTION CLASS 5
;-----;
;
;REGISTER MODE=0: R(N)
;
76  LSOP0:  ILR R0,RG2,JPX DU1RB ;114 AC=R(N)          /00232/  001001100 1111011 0000000 0011 000 1 00 01000011
;
;REGISTER MODE=1: (R(N))+
;
77  LSOP1:  LMI R0,RG2,EGDI,INCR ;115 MAR=R(N), R(N)=R(N)+CONDIN/00236/  001001101 0000111 0010000 0011 100 1 00 10000011
125      ILR R0,1,RG2,DI,PLA7,JMP LSCHR ;R(N)=R(N)+1        /00237/  001111101 0110111 0000000 1111 111 1 00 01000011
;
;REGISTER MODE=2: -(R(N))
;
78  LSOP2:  LMI R0,KAI,RGZ      ;116 R(N)=R(N)-1     /00241/  001001110 0010011 0010000 0011 000 0 00 01000011
318      LMI R0,KAI,RGZ,EINS,DECR ;R(N)=R(N)-1+CONDECR /00242/  100111110 0011101 0010000 0011 011 0 00 11000011
478      LMI R0,RG2,GDI,JMP LSCH1 ;MAR=R(N)           /00243/  111011110 0110111 0010000 0011 000 1 00 00000011
;
;REGISTER MODE=3: X(R(N))
;
79  LSOP3:  LMI R7,1,GWDI       ;117 MAR=R(7), R(7)=R(7)+1. /00247/  001001111 0010110 0010111 1111 000 1 11 00010011
367      ILR R7,1,WDI          ;R(7)=R(7)+1        /00248/  101101111 0111101 0000111 1111 000 1 11 01010011
365      ILR R0,RGZ,WDI        ;AC=R(INZ)          /00249/  101101101 0011000 0000000 0011 000 1 00 01010011
397      AMA AC,PHDI,KAI       ;AC=AC+M(MAR)      /00250/  110001101 0110111 0001011 0011 000 0 11 01110011
391      LMI AC,GDI            ;MAR=AC            /00251/  110000111 0011101 0011101 0011 000 1 11 00000011
471 LSCH1:  NOP PLA7          ;ADDR LINES SETTLE /00252/  111010111 0000111 0001101 0011 111 1 11 01000011
119 LSCHR:  LTM AC,KAI,WIF13,PDIP,JPX DU1RB ;167 AC=M(MAR)      /00253/  001110111 1111011 1011011 0011 010 0 11 01100011
;
120 LS1RB:  NOP SETD1,SETD2,PLAS ;170 JUMP TO INSTRUCTIONS TST. /00255/  001111000 0101100 0001101 0011 101 1 01 00000010
12  LS1B1:  LMI R7,JPX TST     ;14 MAR=PC          /00256/  000001100 1111011 0010111 0011 000 1 11 01000011
;

```

:INDIRECT BIT SET

```

121 LSDEF: LMI AC,GDI ;171 MAR=AC /00260/ 00111001 0110011 0011101 0011 000 1 11 00000011
115 NOP DI,PLAG ;ADDR LINES SETTLE /00261/ 001110011 0000110 0001101 0011 110 1 11 01000011
99 LTH AC,KAI,PDI,JPX DUJRB /00262/ 001100011 1111011 1011011 0011 000 0 11 01100011
;
122 LS0B: LDI AC,1,KAI,PLAS,JPB LS1B1 ;172 000 BYTE - SWAP AC /00264/ 00111010 0101100 0101111 1111 101 0 11 01000011
;

```

```

-----
: TRAP DEFINITIONS START HERE
-----
;

```

```

;PUSH PS ON STACK
;R9 CONTAINS TRAP ADDRESS
;R0 IS USED TO HOLD THE ADDRESS OF THE PSW
;IF Z BIT IS SET, JUMP TO CONSOLE CODE.
;
;JUMP HERE ON ODD ADDRESS AND SSWN TIME OUT
;
248 BETRP: LMI R9,K4 ;370 TRAP TO LOC 4 /00278/ 01111000 0111101 0011001 0011 000 1 11 11101101
253 SDR R0,1 STZ,CLRIT,JZF GTRP1,DBERR /00279/ 01111101 1011111 0101000 1101 000 1 11 10110010
;
;R0=0, TEST AND SET Z BIT
;CLEAR TRACE TRAP F.F.
;
;JUMP HERE FOR ALL OTHER TRAPS
;

```

```

10 GTRAP: ANR R0,0 STZ,CLRIT ;12 R0=0,Z=0,CLEAR TRACE TRAP F /00285/ 000001010 0001111 1001000 0001 000 1 11 10110010
250 GTRP1: LMI R0,KL1,KM11,KNZ ;372 R0=MAR=177776 /00286/ 011111010 0000010 0011000 0011 000 0 00 00000101
42 AMA AC,GPWDI ;412 AC=M(177776) /00287/ 000101010 0111000 0001011 0011 000 1 11 00110011
40 LMI R0,KL1,KM11,KNZ ;400 R0=R0-2 /00288/ 000101000 0011100 0010110 0011 000 0 00 00000101
456 LMI R0,EINS,STKOV ;401 MAR=R0 /00289/ 111001000 0011110 0010110 0011 111 1 11 11000011
488 NOP ;403 WAIT FOR RED ZONE STACK /00290/ 111101000 0011111 0001101 0011 000 1 11 01000011
;
;OVERFLOW MICRO INTERRUPT
;
504 NOP GWDD ;404 WAIT FOR TRAP /00292/ 111111000 0111101 0001101 0011 000 1 11 00011011
509 NOP PWDD ; M(R0)=PS /00293/ 111111101 0110101 0001101 0011 000 1 11 01111011
;
;PUSH PC ON STACK
;

```

```

501 LMI R0,KL1,KM11,KNZ ;405 R0=R0-2 /00297/ 111110101 0110000 0010110 0011 000 0 00 00000101
496 LMI R0,EINS,STKOV ;406 MAR=R0 /00298/ 111110000 0010011 0010110 0011 111 1 11 11000011
304 NOP ;407 WAIT FOR RED ZONE STACK /00299/ 100110000 0110110 0001101 0011 000 1 11 01000011
;
;OVERFLOW MICRO INTERRUPT.
;
310 TSVPC: ILR R7,GWDD ;667 M(R0)=PC /00301/ 100110110 0010000 0000111 0011 000 1 11 00011011
262 NOP PWDD ;66Z WAIT FOR BUS /00302/ 100000110 0110100 0001101 0011 000 1 11 01111011
;
;PICK UP NEW PC
;POWER FAIL TRAP ENTERS HERE
;

```

```

260 PFTRP: LMI R0,1,GWDD ;404 MAR=R0,R0=R0+1 /00307/ 100000100 0110111 0011001 1111 000 1 11 00010011
263 ADR R0,1,WDI ;R0=R0+1 /00308/ 100000111 0111111 0111001 1111 000 1 11 01010011
271 AMA AC,PWDI ;AC=M(MAR) /00309/ 100001111 0001101 0001011 0011 000 1 11 01110011
223 SDR R7,1,KAI ;R7=AC /00310/ 011011111 0001001 0100111 1111 000 0 11 01000011
;
;PICK UP NEW PS
;

```

```

159 LMI R0,GWDD ;MAR=R0 /00314/ 010011111 0111110 0011001 0011 000 1 11 00010011
158 AMA AC,PWDI ;AC=NEW PS /00315/ 010011110 0010010 0001011 0011 000 1 11 01110011
302 LMI R0,GWDD ;MAR=PSW /00316/ 100101110 0010111 0011000 0011 000 1 11 00011011
302 SDR R0,1,PWDD,JPB FETCH ;R0=0; SET PSW /00317/ 101111110 0101011 0101001 1111 000 1 11 01111011
;

```

```

;DOUBLE BUS ERROR WHEN DOING A TRAP, OR BUS
;ERROR WHEN IN CONSOLE MODE.
;

```

```

251 DBERR: ANR R0 /00322/ 011111011 0111110 1001001 0011 000 1 11 01000011
254 LMI R0,KTPS,KL1,KTY ;373 MAR=PUNCH STATUS REG /00323/ 011111110 0001110 0011001 0011 000 0 10 00101101
;
;OUTPUT A "?" AND JUMP TO
;CONSOLE.
;

```

```

230 OUTOM: AMA AC,GPWDI,JFL TSTOM,QMRDY ;PUNCH READY /00325/ 011101110 1001110 0001011 0011 000 1 11 00110011
234 TSTOM: TZR AC,KM10,K0,JPB OUTOM /00327/ 011101010 0111110 1011101 0011 000 1 01 11111011
235 QMRDY: ANR AC /00328/ 011101011 0110111 1001101 0011 000 1 11 01000011
231 LMI AC,KOM ;AC=??? /00329/ 011100111 0111100 0011101 0011 000 1 11 00000001
236 LMI R0,KTPB,KL1,KTY ;MAR=PUNCH /00330/ 011101100 0111101 0011001 0011 000 0 10 00100101
237 ANR R0,GPWDD,JPB CONSL ;OUTPUT BUFFER /00331/ 011101101 0101110 1001001 0011 000 1 11 00111011
;
;

```

```

-----
: INSTRUCTION DEFINITIONS START HERE
-----
;

```

```

;SPECIAL CODE TO MAKE MOV, CMP, ADD, AND SUB RR MODE GO FAST
;

```

```

84 MOVRR: ILR R0,R01 ;AC=S /00342/ 001010100 0011000 0000000 0011 000 1 10 01000011
300 NOP SMOV1,SMOV2,JPB WDESRR ;MAR=PC,SET PSW /00343/ 110000100 0000000 0001101 0011 000 1 01 00101110
;
85 CMPRR: ILR R0,R02,EGWDD ;AC=D /00345/ 001010101 0011010 0000000 0011 000 1 00 10010011
;

```



```

482 SECL1: CIA AC,GWDIP          ;742 AC=NOT AC          /00434/ 111100010 0111001 0011111 0011 000 1 11 00010111
489 ANM AC,KAI,PWDIP,JMP SEZ    ;442 AC=AC AND PS      /00435/ 111101001 0110101 1001011 0011 000 0 11 01110111
;
; SET CC
483 SECL2: ORM AC,KAI,GWDIP      ;743 AC=AC OR PS      /00438/ 111100011 0110101 1101011 0011 000 0 11 00110111
485 SEZ: SDR R9.1,JMP WDESX      ;443 563 R9=0         /00439/ 111100101 0100000 0101001 1111 000 1 11 01000011
;
100 ENT: LMI R9,K30,JZR GTRAP    ;TRAP TO LOC 30       /00441/ 001100100 0101010 0011001 0011 000 1 11 10011101
;
101 TRAP: LMI R9,K34,JZR GTRAP    ;145 TRAP TO LOC 34   /00443/ 001100101 0101010 0011001 0011 000 1 11 10001101
;
103 SOB: ILR R0,PG1              ;147 AC=R(N)          /00445/ 001100111 0011001 0000000 0011 000 1 10 01000011
407 SDR R0,PG1,KAI              ;627 R(N)=AC-1        /00446/ 110010111 0011111 0100000 0011 000 0 10 01000011
503 TZR R0,PG1,KAI              ;622 R(N) ZERO?       /00447/ 111110111 0111110 1010000 0011 000 0 10 01000011
510 ILR T,JFL SDBR0,SDBR1        ;462 AC=T...JUMP FOR ZERO /00448/ 111111110 1001010 0001100 0011 000 1 11 01000011
426 SDBR0: LMI R7,EGWDI,JMP FFET ;503 NO.GO TO FETCH    /00449/ 110101010 0100111 0010111 0011 000 1 11 10010011
427 SDBR1: TZR AC,KM90,K77        ;502 AC=AC AND 77      /00450/ 110101011 0110000 1011101 0011 000 1 11 00000001
416 CIA AC.1,JMP BRNEG          ;AC=-(AC)             /00451/ 110100000 0011100 0011111 1111 000 1 11 01000011
;
20 ROR: SRA AC,SROR1,SRORZ,JPX 0 ;DO A ROR              /00453/ 000010100 1111000 0001111 0011 000 1 11 01010110
;
21 ROL: ILR AC,KAI,SROL1,SROLZ,JPX 0 ;DO A ROL              /00455/ 000010101 1111000 0001101 0011 000 0 11 11010110
;
22 ASR: SRA AC,SASR1,SASRZ,JPX 0 ;DO A ASR              /00457/ 000010110 1111000 0001111 0011 000 1 11 01001110
;
23 ASL: ILR AC,KAI,SASL1,SASLZ,JPX 0 ;DO A ASL              /00459/ 000010111 1111000 0001101 0011 000 0 11 11000110
;
89 RTS: ILR R0,PG2              ;AC=R(N)              /00461/ 001011001 0010111 0000000 0011 000 1 00 01000011
377 SDR R7.1,KAI                ;R7=AC                /00462/ 101111001 0011000 0100111 1111 000 0 11 01000011
;PDP TOP ELEMENT OFF OF STACK
393 LMI R6.1,GWDI                ;MAR=R6,R6=R6+1       /00464/ 110001001 0011010 0010110 1111 000 1 11 00010011
425 ADR R6.1,WDI                ;R6=R6+1              /00465/ 110101001 0111000 0110110 1111 000 1 11 01010011
424 AMA AC,PWDI                ;AC=H(MAR)            /00466/ 110101000 0110111 0001011 0011 000 1 11 01110011
423 SDR R0.1,KAI,PGZ,JZR FETCH  ;R(N)=AC              /00467/ 110100111 0101011 0100000 1111 000 0 00 01000011
;
19 SWAB: LDI AC.1,KAI,SSWB1,SSWBZ ;AC=AC EXCHANGED      /00469/ 000010011 0101000 0101111 1111 000 0 11 10111110
0 NOP SSWB3,JPX 0              ;TO FIX TIMING BUG    /00470/ 000001000 1111000 0001101 0011 000 1 11 00111010
;
18 COM: CIA AC,SCOM1,SCOM2,JPX 0 ;D=NOT D              /00472/ 000010010 1111000 0011111 0011 000 1 01 10101110
;
26 INC: ILR AC.1,SINC1,SINC2,JPX 0 ;D=D+1                /00474/ 000011010 1111000 0001101 1111 000 1 01 00000110
;
27 DEC: SDR AC,KAI,SDEC1,SDEC2,JPX 0 ;D=D-1                /00476/ 000011011 1111000 0101101 0011 000 0 10 00000110
;
28 NEG: CIA AC.1,SNEG1,SNEGZ,JPX 0 ;D=(NOT D)+1         /00478/ 000011100 1111000 0011111 1111 000 1 00 10000110
;
16 AOC: ILR AC,SADC1,SADCZ,JPX 0 ;HARDWARE HANDLES C IN /00480/ 000010000 1111000 0001101 0011 000 1 01 01010110
;
17 SBC: SDR AC,KAI,SSBC1,SSBC2,JPX 0 ;HARDWARE HANDLES C IN /00482/ 000010001 1111000 0101101 0011 000 0 10 10011110
;
24 BIC: CIA T                    ;S=NOT S              /00484/ 000011000 0000011 0011110 0011 000 1 11 01000011
56 ANR T,KAI,JMP MTWD           ;T=(NOT S) AND D      /00485/ 000111000 0111001 1001100 0011 000 0 11 01000011
;
25 BIS: ORR T,KAI                ;T=S OR D             /00487/ 000011001 0000011 1101100 0011 000 0 11 01000011
57 MTWD: ILR T,SBCS1,SBCS2,JPX 0 ;AC=T                 /00488/ 000111001 1111000 0001100 0011 000 1 01 00101110
;
30 ADD: ILR T,KAI,SAOD1,SAODZ,JPX 0 ;D=D+S                /00490/ 000011110 1111000 0001100 0011 000 0 00 01101110
;
31 SUB: SDR R0.1,KAI            ;R0=AC=D              /00492/ 000011111 0010111 0101000 1111 000 0 11 01000011
383 ILR T                    ;AC=T-S              /00493/ 101111111 0011000 0001100 0011 000 1 11 01000011
399 CIA AC                    ;S=NOT S              /00494/ 110001111 0111110 0011111 0011 000 1 11 01000011
398 NOP SETS1,SETS2            /00495/ 110001110 0101111 0001101 0011 000 1 10 00000010
15 ILR R0.1,KAI,SSUB1,SSUBZ,JPX 0 /00496/ 000001111 1111000 0001000 1111 000 0 00 10110110
;
29 XOR: SDR T.1,KAI            ;T=AC                 /00498/ 000011101 0000011 0101100 1111 000 0 11 01000011
61 ILR R0,PG1                  ;AC=R(N)              /00499/ 000111101 0111110 0000000 0011 000 1 10 01000011
62 XNR T,KAI                    ;T=T XOR AC           /00500/ 000111110 0000010 1111100 0011 000 0 11 01000011
46 ILR T                        ;AC=T                 /00501/ 000101110 0111101 0001100 0011 000 1 11 01000011
45 CIA AC, SXOR1, SXORZ, JPX 0 ;S5 AC=NOT AC         /00502/ 000101101 1111000 0011111 0011 000 1 01 00101110
;
33 IJMP: SDR R7.1,KAI,JZR FETCH ;R(7)=D ADDRESS      /00504/ 000100001 0101011 0100111 1111 000 0 11 01000011
;
36 JSR: SDR T.1,KAI            ;T=D ADDRESS, T IS TMP /00506/ 000100100 0010111 0101100 1111 000 0 11 01000011
372 ILR R0,PG1                  ;AC=R(N)              /00507/ 101110100 0110101 0000000 0011 000 1 10 01000011
373 LMI R6,KM2,KL1,KM11         ;R6=R6-2              /00508/ 101110101 0111000 0010110 0011 000 0 00 00000101
376 LMI R6,EINS,STKOV          ;MAR=R(6)             /00509/ 101111000 0011000 0010110 0011 111 1 11 11000011
392 NOP                          ;WAIT FOR RED ZONE STACK /00510/ 110001000 0111100 0001101 0011 000 1 11 01000011
;
396 NOP GWDG                    /00512/ 110001100 0011001 0001101 0011 000 1 11 00011011
412 NOP PHDD                    /00513/ 110011100 0011010 0001101 0011 000 1 11 01111011
420 LMI T                        ;MAR=NEXT PC         /00514/ 110101100 0111110 0011100 0011 000 1 11 01000011
430 ILR R7,EGWDI                ;AC=R7                /00515/ 110101110 0111111 0000111 0011 000 1 11 10010011
431 SDR R0.1,KAI,PG1            ;R(N)=R7              /00516/ 110101111 0011011 0100000 1111 000 0 10 01000011
447 ILR T                        ;AC=T(TMP)           /00517/ 110111111 0111110 0001100 0011 000 1 11 01000011
446 SDR R7.1,KAI,JMP FFET       ;R7=TMP               /00518/ 110111110 0100111 0100111 1111 000 0 11 01000011
;
34 CLR: TZR AC,SCLR1,SCLRZ,JPX 0 ;42 D=0               /00520/ 000100010 1111000 1011101 0011 000 1 01 01101110
;

```