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Final Report

ANALOG AUTOMATIC TEST PROGRAM GENERATION USING NOPAL

by

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This is a study of analog automatic test program generation
>erformed in the context of the NOPAL system. The purpose
>f the research undertaken was to use the NOPAL system to generat
LTLAS language programs to test analog circuit cards with the
IQUATE (AN/USM-410) Automatic test equipment.

The software system is composed of top and bottom parts,
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:ircuit description of an* analog circuit. The bottom part
generates EQUATE ATLAS programs from nonprocedural specifications

In this report both the top and the bottom parts of the NOPA
system are used together to generate test programs to diagnose
md isolate single catastrophic failures on two different circuit
:ards taken from the AN/VRO12 radio set. The complete process
>f describing the circuit cards to the NOPAL System, generation
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presented and evaluated.

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CHAPTER I

Introduction

This is a study of analog automatic test program generation process performed in the context of the NOPAL system. The purpose of the research undertaken was to use the NOPAL system to generate programs in the ATLAS language to test analog circuits using an automatic test equipment. This software system is composed of top and bottom parts. The top part relates to the generation of nonprocedural test specifications from the description of an analog circuit. [1] The bottom part relates to the generation of ATLAS programs from a nonprocedural specification.[2] Both parts can be used independently of each other. A list of relevant reports and papers published by the NOPAL project is included in the references.

The effectiveness of the NOPAL system was investigated by taking two separate approaches. In one case only the bottom part was used to generate ATLAS programs to program the perform tests on the AN/ARC-114 radio set. The description of the test was taken directly from the depot maintenance work requiremen documents and written by hand in the NOPAL specification langua All tests were successfully conducted on the EQUATE test equipment. The findings of this approach are presented in a separate report. [3]

In the second case, both the top and the bottom parts of the NOPAL system were employed together to generate programs to diagnose and isolate failures on two different circuit cards taken from the AN/VRC-12 radio set. In this report the complete process of describing the circuit cards t the NOPAL system, generation of intermediate tables, the test specifications, and the ATLAS programs are described. Finally examples from actual ATE runs are presented and evalu.

The report is organized in six chapters. Chapter I is a the contents and organization of this report.

Chapter II provides a description of our overall approac analog automatic test program generation based on our past re and development activity. Sufficient detail is provided so a to obviate the need for frequent reference to the earlier tec publications and related documentation.

The modelling of circuit components and ATE devices are described in Chapter III. The variety of circuit components, failure modes, stimulus and measurement devices is limited to those types utilized in the test program generation for the A. and A5100 circuit cards. A description of interfacing these circuit cards to the EQUATE is also provided.

The complete process of test program generation and execution to diagnose and isolate single catastrophic failures in the A2100 card is described in Chapter IV. A description of the input supplied to the top part of the NOPA system is followed by an overview of the tables generated by

the system. The specification of tests based on these tables is also explained. Finally, the ATLAS program generated from these tests is described and followed by program execution results.

A description of test program generation for the A5100 circuit is given in Chapter V. The organization of this chap follows closely the previous chapter.

A summary of the findings of this research, success and difficulty areas encountered in using NOPAL, and suggestions for future research and improvements are given in the final Chapter VI.

The appendix at the end contains the semiconductor models in the circuit analysis language used in this work. It can be used as reference to build models for other devices

CHAPTER II

An Overview of the NOPAL Approach To Analog Automatic Test Program Generation

2.1 General Approach

This section provides a description of our overall approach to analog automatic test program generation (AATPG) based on our past research and development activity. Sufficie detail is provided so as to obviate the need for frequent reference to the earlier technical publications and related documentation.

We have developed an AATPG system, called the NOPAL system, which automatically generates programs in the ATLAS test programming language to test and diagnose malfunctions in analog electronic circuit boards. The system consists of two distinct parts: a <u>top-part</u> which analyzes the circuit diagram and determines the necessary tests, and a <u>bottom-part</u> which analyzes the required tests and produces a program in the RCA EQUATE ATLAS test language for use with the RCA AN/USM automatic test equipment.

The top-part, the NOPAL language, and the bottom-part are described in respective subsections below.

The application of computer technology to automated testing of electronic circuits should suggest not only the use of computers but also the employment of automatic programming methodologies. The tasks of developing functional or fault diagnosis tests, and the programming of computer controlled test equipment to perform these tests are strikingly similar

to software development tasks in many other areas of applicat of computers. Recent research on automatic generation of computer programs has been motivated by the high costs and expertise needed for software development. These same proble exist in automatic testing as well. The complete automatic performance of these tasks seems the only effective way to reduce significantly the required costs and expertise. Our work to date applies automatic program generation methods to testing of analog electronic circuits. It consists of structuring and incorporating the methods of analysis of electronic circuits and the methods of computer programming within an automatic system named NOPAL, which performs the software development for testing a specified circuit by compu controlled test equipment.

Software development is generally characterized as a three-phase procedure consisting of (1) development of requir ments, (2) development of a specification for each program unit, and finally (3) development of each program in a high level language, A similar approach is generally used in automatic program generation systems which consist of two par (1) a <u>top-part</u> which accepts as input a statement of problem requirements and produces, as an output, a program specificat and (2) a <u>bottom-part</u> which accepts, as input, the program specification, and produces a program in a high level languag

This general approach has been adopted in NOPAL. The top-part of NOPAL analyzes the circuit to be tested and produ a specification of the needed set of tests (expressed in the NOPAL language), The top-part is based primarily on knowledg

of electronic circuits and systems. It is approximately 16,000 FORTRAN statements long. The bottom-part performs the computer programming task and produces a program in t ATLAS test language. It is based primarily on programmin knowledge.

As illustrated in Figure 2.1, information consisting of circuit diagrams, circuit layout and testing objective is evaluated in the top-part. Necessary changes in the design are indicated when testing cannot satisfy the requ ments. If the design is satisfactory, the top-part of th system can determine a complete set of functional and fau isolation tests to be employed in fabrication and mainten The bottom-part, consisting of approximately 18,000 lines of PL/1 code, produces a corresponding ATLAS program that is utilized in computer controlled automatic test equipme which will test the unit under test (UUT) and produce app diagnoses.

Each of these two parts is independent of the other could be usefully employed by itself. The interface betw the top and bottom parts is a specification of tests expr in a language named NOPAL. Unlike ATLAS, NOPAL is not a programming language. It is a <u>specification language</u> in sense that it can be used only to describe individual tes It does not have facilities for stating commands or for sequencing the execution of tests. The top-part may be u by itself, where the user writes the test programs manual based on the automatically produced test specifications.

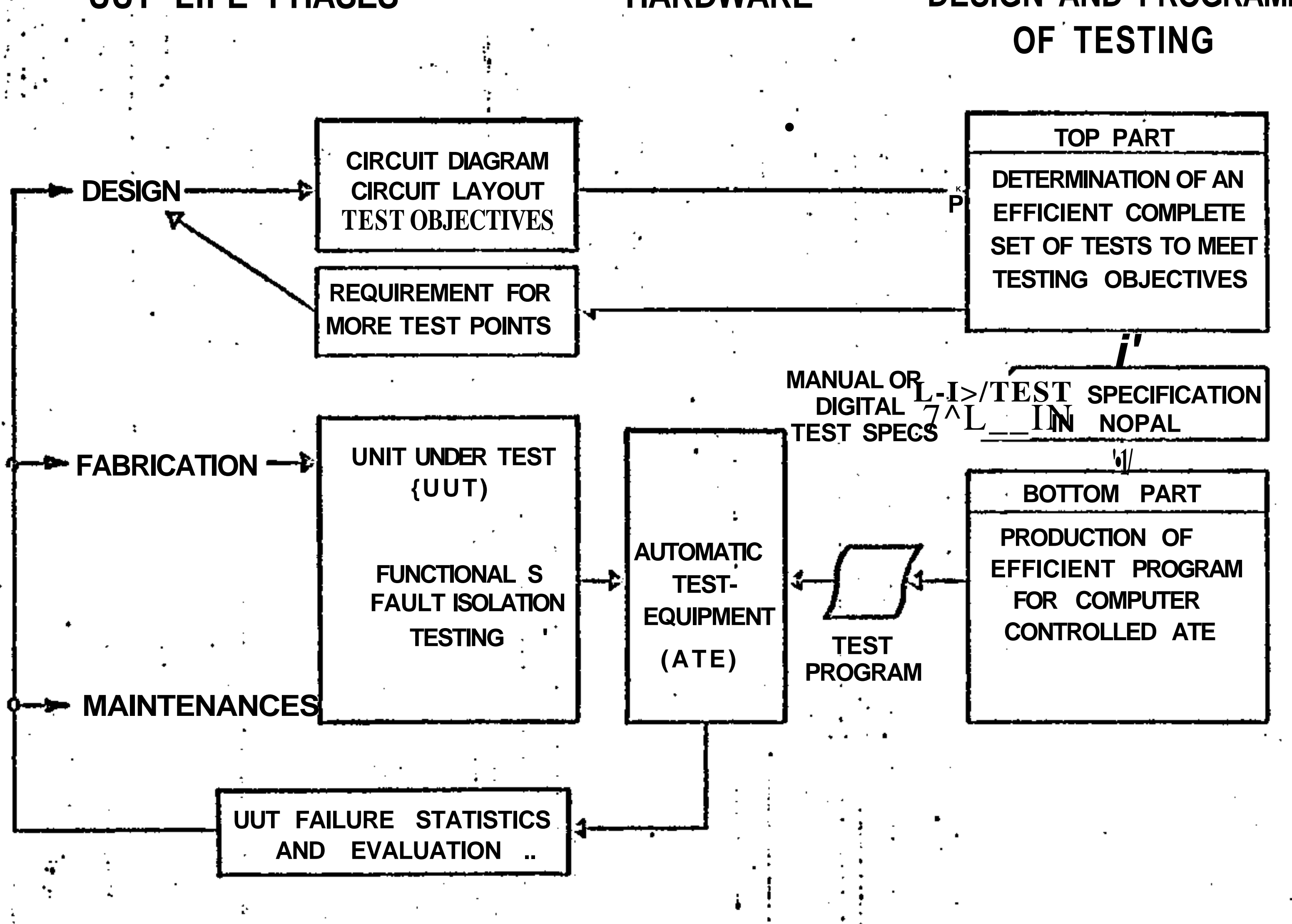


FIGURE 2.1 IH:SKN AND USB OF TESTING IN TIE LIFE CYCLE OF A WIT INDER TEST *(UUT)*

can also be specified in NOPAL manually in which case only
bottom-part of the system is utilized to generate the ATLAS
programs.

In the following, the top-part is described first, and
followed by a description of the bottom-part.

The NOPAL system described is oriented towards the RCA
EQUATE ATLAS[4] test language and the associated complemen
of test equipment. However, the system incorporates featur
that facilitate production of programs in other test pro-
gramming languages and different computer controlled test
equipment.

2.2 Design For Automatic Testing: The Top Part Of Nopal

The objective of the top-part of the system is to find
a small and effective set of tests for a UUT, and express i
in the NOPAL language. The process is illustrated in Figur
The input required for the user is shown on the left side
of Figure 2.2 and described in subsection 2.2.1. The
methodology and processes are shown at the center of Figure
and are described in section 2.3. The output reports are
shown on the right of Figure 2.2 and are described in
subsection 2.4. The NOPAL language, in which the tests are
specified, is described in subsection 2.5.

There are six input sections: (1) circuit description
(2) accessible test terminals, (3) UUT failure definitions,
(4) fault isolation testing objectives, (5) measurement
accuracy, and (6) initial conditions. The first input is r

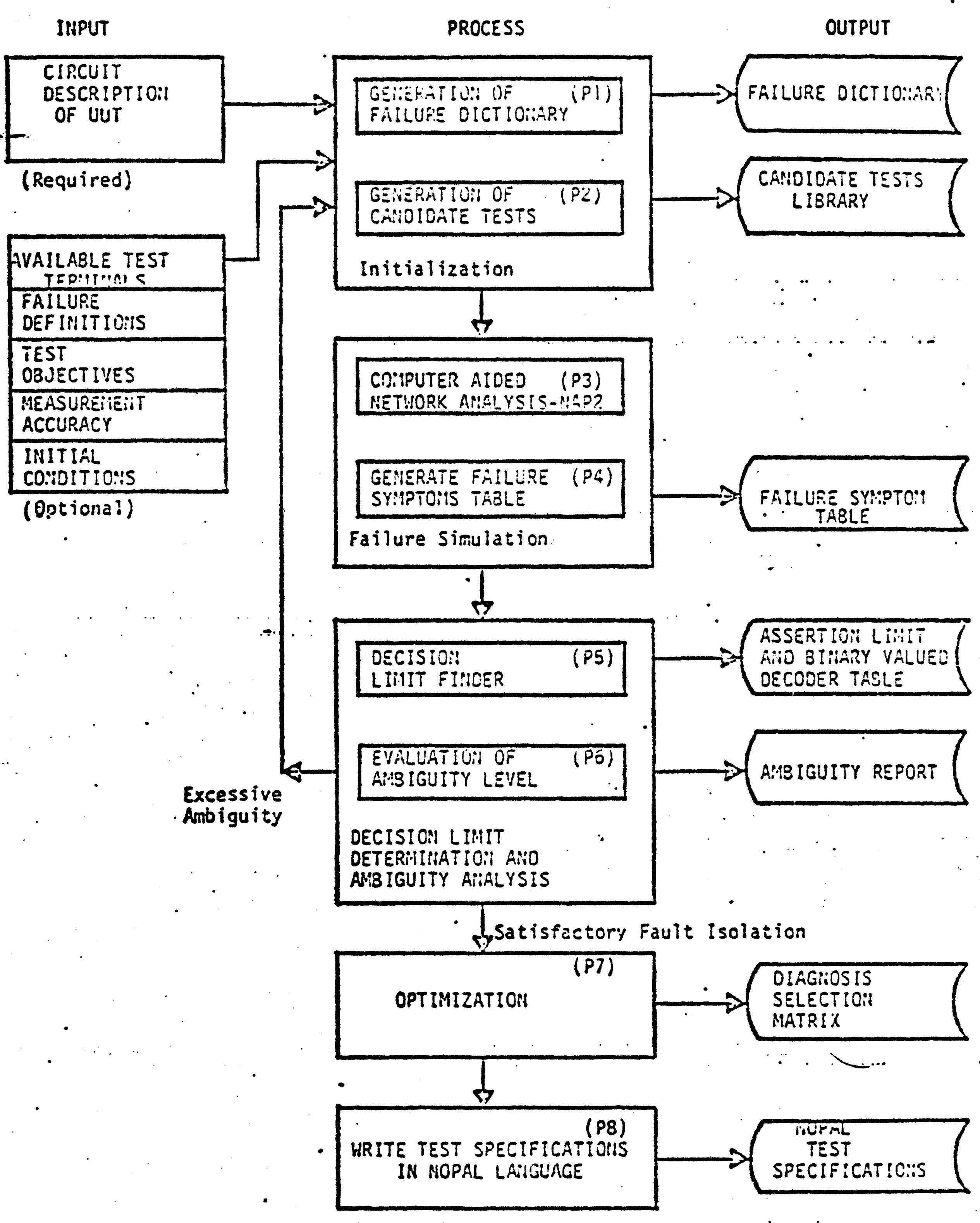


FIGURE 2:2 FLOWCHART OF TOP PART OF NOPAL SYSTEM

id the remaining are optional. They are all important to understanding te test design process.

<u>Circuit Description of UUT</u>: The test design is based on modeling and .mulation of the UUT under nominal and malfunctioning conditions for determini le symptoms of component failures. The analysis of the circuit in the top-par i based on simulation of faults. The modeling is based on the equivalent cir- lit drawing of the UUT, The equivalent circuit may consist of resistors, capa Ltors, inductors, mutual-inductances, voltage and current sources, bipolar and ST devices. Accurate modeling of the last two component types may be an invol isk, however sufficient published data is available for popular types. Each Lrcuit component is given a unique name, where first letter identifies the jmponent type. The value of any element may be defined by a numerical constan *ble, or mathematical expression. Component tolerances are specified by tating the maximum percentage deviation from the nominal value. Each circuit Dde is ..assigned a name. Current flow direction and source polarities are also adicated. The status of mechanical switches or potentiometers are treated as ifferent initial conditions of the system. The description of an equivalent ircuit follows conventions used in Computer Aided Circuit Analysis (CANA) pro- rams. We use the NAP 2 CANA program and follow its conventions,[5]

<u>Availability of Test Terminals</u>: Any of the circuit nodes may be used for ttaching test devices. However, the user may restrict the class of terminals vailable for testing to external contacts on the circuit board. Manual probe ontact points may also be specified.

<u>Failure Definition</u>: The objective of testing is to discover the componeni f the UUT that have failed in a manner defined by the user. Since failure is ... any deviation from a component's nominal value may be declar

the user to be a failure. Failure definitions may include topological chang
ch as the removal or addition of a component. Typically catastrophic (open
d short circuit) and out-of-tolerance failures are most common. To ease the
sks of input preparation, individual catastrophic failures are included autom
cally and the user has to declare only the remaining failure definitions (i.e.
ltiple component failures) as changes to the nominal circuit description. The
nber of tests that are required is related to the number of failures. Testing
agnose a large number of potential faults may be extremely time consuming and
nsive. The user can compromise between cost and quality by restricting the
st objectives to discover only the more likely or most harmful failures.

Fault Isolation Test Objectives: To reduce the number of tests and lower
sting costs, the user may wish to accept tests which will sometimes not locat
failure in a specific component, but in a small group of components. The
ilure isolation requirement is expressed in statements denoting that P_k% of t
tal number of possible failures may be located in ambiguous classes consistin
k or less components. P's are cumulative percentages, therefore $P_{k_1} < P_{k_2}$
n and $k_1 < k_2$---k_n.

Measurement Accuracy: Three types of accuracy may be specified (1) minimum
asurement threshold, (2) percentage inaccuracy of the measurement, (3) number
significant digits of the measured value. The default values are 0.1% measu
nt scale inaccuracy and four significant digits in the meter readings. All
its are in MKS.

Initial Conditions: A final optional input section specifies also the
itial conditions of the UUT to speed the computer solution.

METHODOLOGY AND PROCESS OF TEST DESIGN

As shown in Figure2.2 the first component of the process (P1) creates a
ilure dictionary data base for the UUT, based on the UUT circuit and failure

scription supplied in the input.

The next component (P2) generates candidate stimuli and measurements for sts using the three strategies described below, one at a time. First, small ltage stimuli (d.c. or a.c., depending on the type of components involved) ar nnected to connecting - points of the UUT, with the objective of measuring pedances at the connection points. This is referred to as the cold-circuit rategy. Next, the UUT is powered with the nominally specified d.c. power sou d voltage and current measurements are conducted at the available nodes. Thi rategy is referred to as a d.c.-nominal. Finally, an a.c. signal is applied put connecting points and user specified tests are conducted. This strategy ferred to as a.c.-signal. The system design process provides for addition of re test strategies in the future. These strategies are all employed one at a me in the above order.

Next in (P3), the circuit behavior is simulated with the above stimulus plied, with the components having nominal values and with the components havi ilure conditions enumerated in the failure dictionary, one at a time. The nsitivity of the circuit response due to tolerances is also determined for ch case. A CANA program, NAP2 has been selected to perform the simulation sed on considerations of economy of computer usage costs. The simulation oduces, for the nominal case and for each failure, ranges of measurable phys- al entities (voltage, current, phase etc.,) observed at connecting points.

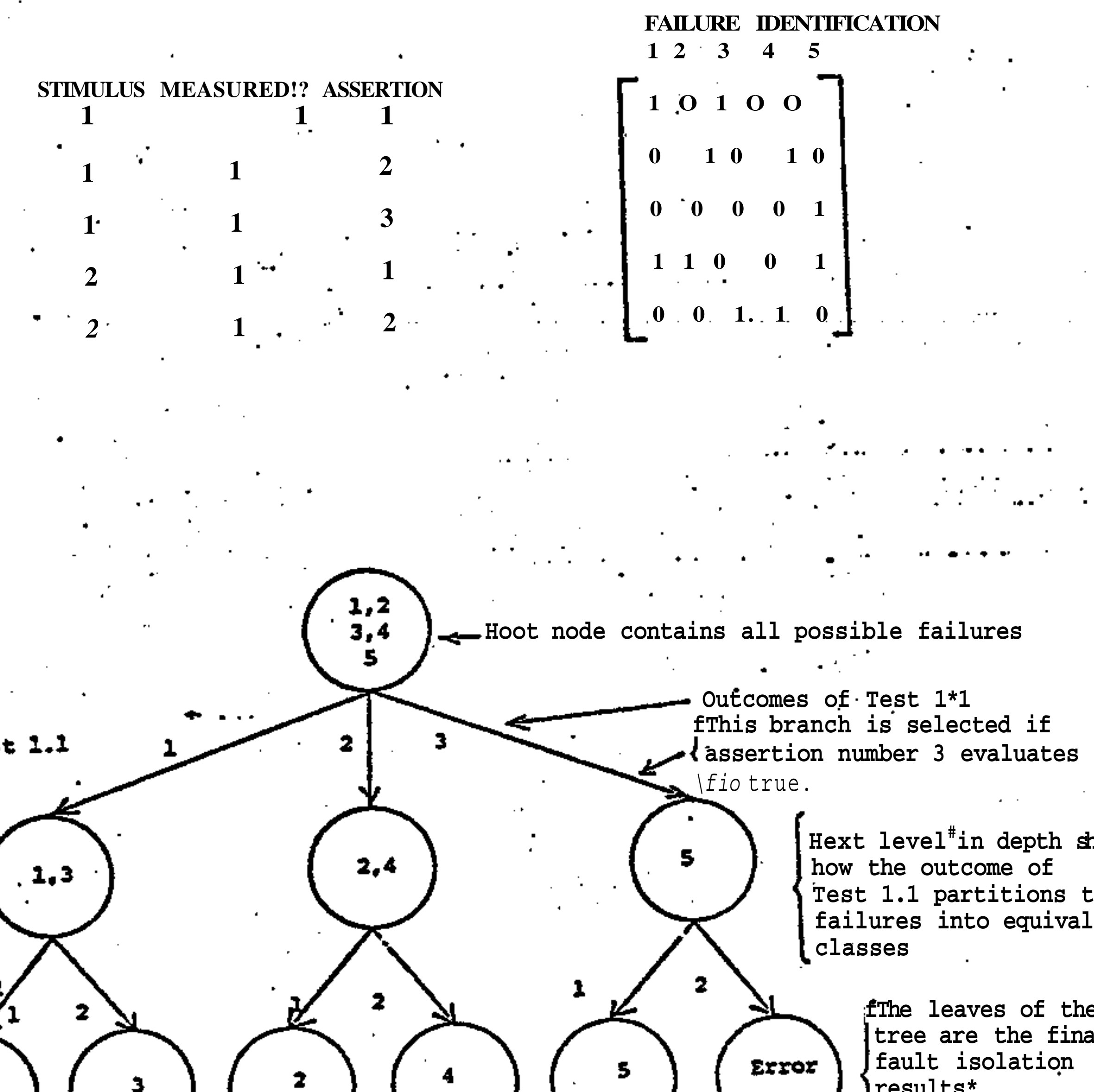
In the 4th component (P4), each range to be verified by a measurement is ecified in an assertion. These assertions, together with information on the sociated connecting points for the stimulus and measurement and on the associ ilures are inserted into a Failure Symptom Table. This is further discussed

Based on this information, it is possible (in P5 and P6 of Figure 2.2) to

rify if the tests formulated so far meet the ambiguity requirement statements t forth in the input. If testing objectives are still not met, the next rategy is employed, new tests are examined and the circuit is simulated until e above criterion is met, or until all three test strategies have been exhaust When it is determined that the ambiguity levels of fault isolation are sati ed, the P7 component (see Figure 2.2) is initiated. The purpose of Process P7 to reduce the number of tests to be performed without loss of fault diagnosis d isolation capability. There are three optimization steps. First, the total mber of test setups is minimized since setup for a test consumes the longest me in actual testing. Second, the available assertions of the remaining tests e further reduced. Finally, diagnosis selection logic statements are found ch that only the minimum number of tests in the remaining set are performed to agnose and isolate each failure or group of equivalent failures.

The first two considerations are attained by the same algorithm. The proach is to create a fault isolation tree. Figure 2.3 illustrates the constr on of such a tree. The top of Figure 2.3 shows the relation of five tests to ve failures. The tests are listed in respective rows. Each test specificatio nsists of three parts, the stimulus, the measurement and the assertion that fines the upper and lower limits. These three parts are identified by numeral r brevity. Thus for instance: 1.2.3. means the combination of the first stimu s, second measurement and third assertion. The failures correspond to respect vs at the top right of Figure 2.3. They are identified by numerals 1 to 5. The trix consists of "1" in positions where a test may identify a corresponding ilure, and "0" in the other positions.

The nodes of the fault isolation tree at the bottom of Figure 2.3 represent e failures as determined by the outcomes of tests. The branches coming out of



STIMULUS	MEASURED!?	ASSERTION
1	1	1
1	1	2
1	1	3
2	1	1
2	1	2

FAILURE IDENTIFICATION

1	2	3	4	5
1	O	1	O	O
0	1	0	1	0
0	0	0	0	1
1	1	0	0	1
0	0	1	1	0

FIGURE 2.3 pAyr,T ISOLATION TREE ILLUSTRATING OPTIMIZATION OF TEST SETUPS AND ASSERTIONS

ach node are labelled by assertions associated with a test setup. Each brand inks to a lower level node containing a disjoint subset of the failures presei n the parent node.

The leaves of the tree represent the equivalence classes of failures aftei esting is finished. Therefore, the leaves of the tree indicate the final fau: solation achieved. Any one of the failure modes included in each leaf may be he possible cause of the failure of a UUT.

There are many ways to create this tree. The approach taken here is to reate a balanced tree with respect to the number of failures included in each ode; that is, the test at each level is selected so that nearly equal number c ailure modes are isolated at each node of the next depth.

The fault isolation tree is created as follows:

- Initialization: Place the names of all the failure modes of the failure dictionary into the root node.
- Determine which test will be used to define the branches out of the root nc The first test setup to be accepted is the one' that yields the -highest enti (information content). The entropy is defined as:

$$H(T_i) = \Sigma_{j=1}^{n} P_{ij} \text{ Log } P_{ij} \; ; \; P_{ij} = \frac{k_{ij}}{N_f}$$

  k_{ij}* is the number of failure modes diagnosed in the jth equivalence class determined by the outcome of test T_i. A node can fanout to m new nodes where m is the number of assertions of that test setup.
- Find the smaller equivalence classes: Using the diagnosis of the test whic yields the highest entropy, construct the distince equivalence classes (noc at the *next* depth of the tree and label the branches coming from each of tl upper level nodes to the .lower level nodes.

Find the next test with the highest entropy: Given the equivalence classes found in Step 3, find the next test which gives the highest entropy. This e tropy is calculated as defined in Step 2. If there are several tests which give the same entropy, then accept the test which has the lowest average measurement sensitivity.

Check for termination: If the entropy has not increased or all tests have b utilized, then "best" fault isolation possible is reached, therefore, termin Otherwise, repeat starting from Step 3.

The fault isolation tree can then be used to minimize first the number of st setups, then the number of assertions. Next the effect of conjunctions and sjunctions of passing and failing tests is analyzed to improve fault isolation l reduce the number of tests. Redundant tests are then deleted. Finally the iimum number of tests and assertions are joined to select the diagnosis. Deta these algorithms are given in [1].

The last component shown in Figure 2 produces these tests in NOPAL syntax.

REPORTS GENERATED DURING TEST DESIGN

The reports produced by the top-part, shown in Figure 2.2, give a step by s :ture of the progress of circuit analysis and test design. This reporting giv : user sufficient information in order to overcome a variety of problems that r arise. Some of these reports are only briefly described below as they are igthy and their understanding would require a detailed explanation of the syst :ch is beyond the scope and space of this paper.

<u>Failure Dictionary</u>: As noted, the failure dictionary consists of the :astrophic failures of the individual components of the circuit and any other :lure modes specified by the user. This report is in the form of a table. Th a row in the table for each failure mode. The columns give: an identificati iber, failure type (open, short, etc.), the nodes of the component in the cir- :t diagram, whether the failure is due to a topological change or due to a

ange in value of a component, the threshold value of the component which indi e failure, the model used to simulate the component and a relative index of kelihood of this failure.

Circuit Analysis Output: This is a data base consisting of the unmodified tputs of the NAP2 system for each simulation of the circuit.

Stimulus, Measurement-region and Failure Tables: This is a series of tabl ich show the tests initially selected and progressively those retained or con ted in the test optimization process, as well as the basis for deletion of ot sts.

Ambiguity Report: An elementary group of failures where it is not possibl distinguish further between the individual (or subgroups of) failures is ref as an equivalent class of failures. This report is in a form of a table wit row for each equivalent class. The columns consist of an identification numb e number of failures (referred to as the ambiguity), the percentage of the to mber of failures, a cumulative percentage, and a list of the component names d their failure functions constituting the equivalence class.

NOPAL Test Specification: This report constitutes the final documentatio the test requirements. The NOPAL test specification itself is shown and ex- ained in the next section. In addition there are several summary reports.

5 INTERMEDIATE LANGUAGE - NOPAL

NOPAL specification statements can appear in any order (due to its non- ocedural nature). Yet, for organization purposes we will consider the tes ecification as divided into the UUT, ATE and Test-Module Sections. Below, e NOPAL specification has been generated automatically by the top-part. We te that the NOPAL language is also easy to use when specifying tests manually.

UUT Specification: consists of two parts, component-failures and test-ter

ATE Specification: ATE related information, which is needed to verify the est Modules and the UUT specifications, is organized in two sections: (1) ATE onnecting points, which are connected to the matching UUT connectors, and 2) ATE functions, which specify evaluation of parameters involving stimulus id measurement devices. Purely computational functions may also be used and Lsted here.

We have allowed the user to define functions, which are high level operaions involving application of stimuli, measurements and computations. These unctions are similar in concept to the use of functions in PL/1. The user wi! Iso be required to specify for each function a procedure in the object languaj f the system (in this case EQUATE ATLAS) utilizing the equipment of the objeci TE unit. These procedures will be further discussed.

Test Module Specification: This section includes a collection of 1) test)dules. 2) diagnoses and 3) messages. The test-modules specification is the < f the NOPAL specification. Each test module is specified independently of the thers, thereby individual test modules can be modified, deleted, or added ithout affecting the rest of the test modules.

The subparts of each test module (in addition to the test module label) a: 1) the stimuli that need to be applied to the UUT at test time, (2) the measuents that need to be made with the comparison limits that will determine the assing or failing of a test, (3) the logic that selects diagnoses based on the esults, and (4) diagnoses. These four parts are described below.

Each test starts with the identification label of the test. The stimuli nd measurements are defined by conjunctions, which specify the devices that mi e applied simultaneously. Each device in a conjunction is specified by a trii hich consists of: 1) the terminals where the device must be connected, 2) a ti elation and 3) the function name (that refers to the device) and the values o

ariable names of the parameters of the function.

Next the assertions specify relations between variables of the tests, sing algebraic and locigal notation in general use.

Finally the logic part of the specification shows the rules for selecting f diagnoses based on the outcome of the test, using notation which implements ult isolation tree described in Section 2.3.

6 AUTOMATIC PROGRAM PRODUCTION: THE BOTTOM-PART OF NOPAL

Figure 2.4 illustrates the components of the automatic program production the NOPAL system. The inputs are test specifications written in NOPAL. [1,7]

The first component in Figure 2.4 performs syntax analysis of the test spec ication. Also, the test specification is encoded and stored in a simulated as ociative memory to facilitate later processing. Syntactical errors and docume ation consisting of a specification listing and several cross reference report ormatted for easy readability, are produced. This component is not described rther here.

The second component incorporates an engineering knowledge-base which is termine and optimize the sequence of execution. In the course of analysis, e system produces various additional reports including error/warnings of dete consistencies, fault locating summary, and a flowchart showing the test execu on sequence. This component incorporates some novel methods and is described rther below in Section 2.7.

The third component generates a test program in EQUATE ATLAS acceptable to RCA AN/USM-410 series ATE. It is briefly reviewed in section 2.8 The objec ogram needs to be compiled by the EQUATE ATLAS compiler, and then it will be ady to test the given class of UUT's.

.7 TEST SEQUENCING AND OPTIMIZATION

The automatic sequencing and optimization process is further discussed

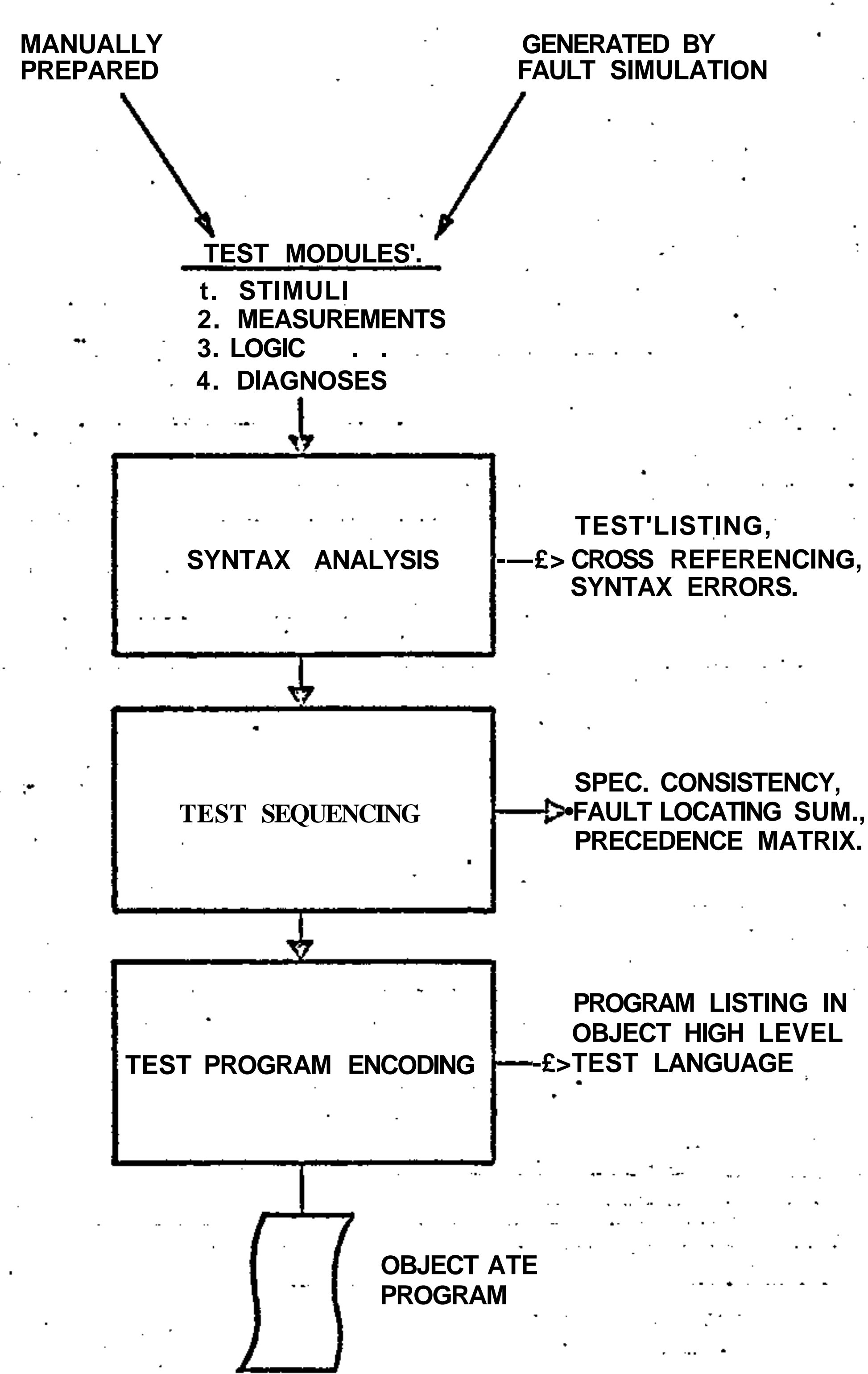


FIGURE 2.4 COMPONENTS OF AUTOMATIC PROCRAH CENERATINC SYSTEM

elow because of its importance and novelty. The NOPAL system automatically ptimizes intra-test and inter-test execution sequences and generates control ogic for dynamically evaluating the conditions that determine the progress of he testing and selection of the next test. The process of determining the equencing consists of considering the test modules and their subcomponents as ntegral units represented by nodes in a directed graph. The specification is nalyzed to determine precedence relationships between test modules or their ubcomponents. These precedence relationships are represented by directed dges in a directed graph. A precedence relationship means that one node must recede the other at execution time of the object test program. One node is a redecessor of the other, which is the successor. Six major inter-test preced elationships are briefly explained in the following.

(1) Data determinacy incorporates the principle that data or variables m e evaluated before they can be used. The generation of data by a predecessor odule is recognized by the declaration of a TARGET variable. A successor est module references the same variable, declared as SOURCE.

(2) Interactiveness relationships are dictated by the need to exchange essages interactively with the ATE operator.

(3) Component protection is based on the concept that non-destructive esting can be achieved if a critical component is tested before other com- onents which depend on it for their normal operation. Furthermore, the failur f such a critical component will prohibit the performance of any test which ha rotected components.

(4) Fault-isolation strategy schedules tests in a top-down fashion using omponent subset relationships. The more generic fault isolation tests are pe ormed first. The lower level, more specific tests are then executed or skipp

epending upon whether the failure is detected at the top level. (similar in c
ept to the tree in Figure 2.3.

(5) <u>Stimuli application</u> is concerned with efficient application of stimul
: is based on the assumption that application of stimuli is most time consumin
ence it is advisable to conduct all the possible tests once a stimulus is appl

(6) <u>Failure likelihood</u> uses the idea that efficiency is obtained by first
esting those components which are more likely to fail. Information is extract
rom the failure index field in the UUT Component Failures specification.

Based on the graph, the consistency, completeness, ambiguity and feasibili
f the test specifications may be checked. Possible cycles in the directed gra
mply errors. They are detected and reported to the user. Finally all nodes a
rdered in proper execution sequence defining a flowchart of the program.

This phase of the system produces two flowcharts showing the order of the
n the object program. The inter-test flowchart report shows the sequence of e
ithin each test module. The intra-test flowchart report shows the overall exe
ion sequence of the test modules.

8 ATLAS CODE GENERATION

The object program may be viewed as constructed in three levels. The two
op levels are generated automatically. The first level is the global program.
: consists of the data declarations followed by calls on procedures for perfor
ing the respective test. It is based on the inter-test flowchart report gener
n the test sequencing phase. Each test is followed by the logic to determine
election of the next test based on the result (passing or failing) of the
revious tests.

The second level consists of procedures for each one of the test modules.
hese procedures are based on respective intra-test flowchart reports generated
n the previous test sequencing phase. Because of limited space these more
engthy procedures are not shown here.

To employ the stimuli and measurement devices, the test procedures include calls on the lower level procedures that correspond to the functions which were specified at the ATE Function section of the NOPAL specification• These procedures are written manually and placed in the Function Library of NOPAL,

The intent of automatic program generation is to keep the user away from the object programming language. The users of NOPAL need not even read the ATLAS code generated. However for system debugging purposes this code may be easily read and understood. By selecting the proper options at the time NOPAL is invoked, an ATLAS program with full program execution trace can be generated. In this mode, the ATE prints the procedures invoked, steps executed, variables computed, and the state of the diagnosis selection process. This mode of operation greatly enhances the user's confidence level in using such automatically generated programs.

It was founid desirable to incorporate in NOPAL various facili that would facilitate its wider use. There is a need for two types of capabilities: first to produce test programs in a variety of high level test languages, and second to incorporate in the produced programs use of stimulus and measuring devices that are available in the automatic test equipment to which the produced programs are oriented. The facilities to attain these two capabilities in NOPAL are as follows:

(1) All except one on the NOPAL system components are independent of the object high level test language in which the programs are to be produced. The only component of the system that is dependent on the test programming language is the Code Generation component shown at the bottom of Figure 2.4. Furthermo this component incorporates tables which translate the entries in the flowchar

(produced by the Test Sequencing component shown in Figure 2.4), into respective test programming language statements. To produce programs in a language other than the EQUATE ATLAS, it would be necessary only to modify the Code Generation component of the system. It is anticipated that the modifications required would not be very difficult due to the tabular structures in this component.

(2) As already noted in the discussion of the NOPAL language, the NOPAL specification has an ATE section where stimulus and measurement device that are to be utilized may be described. The NOPAL system includes a library of routines, in the object test programming language, which correspo to the devices specified in the ATE section of the NOPAL specification. Thus expected use of additional or different devices may be incorporated in the program by entering in the library of the NOPAL system appropriate routi for these devices. This feature also allows for further enhancement by use in the NOPAL specification of very high level and complex devices, which in fact require a simplified model comprised of a number of lower level real devices to perform the equivalent function. This capability allows the use of higher level statements, thereby saving much labor by the user.

CHAPTER III

Modelling of Circuit Components and ATE Devices

3.1 Semiconductor modelling

The NOPAL approach to fault diagnosis and isolation is based on simulation of the circuit to be tested with its components in the nominal and failed modes. The stimulus and measurement functions (effectively ATE devices) are included in the simulation. In some cases the signals between the circuit and test equipment pass though an interface device. If this is the case, a circuit equivalent description of the interconnecting device is included in the simulation. The models used in the simulations are described in this chapter.

In Section 1 of this chapter, modelling of the semiconductor devices in the NAP2 circuit analysis language is described. The semiconductor device types are limited only to those found on the A2100 and A5100 circuit cards. In Section 2 models of other circuit components and equivalent circuit diagrams of single component failures are described. The modelling of ATE stimulus and measurement devices are described in Section 3. The variety of stimulus measurement device models presented in this chapter is limited to those devices of the EQUATE used in testing the A2100 and A5100 circuit cards. The ATE-UUT interconnecting devic for the above cards is described in Section 4.

A. Diode Model

Because of the non-linear V-I characteristics of the diode, correct analysis of a circuit containing diodes becomes criticall dependent on the definition of diode characteristics. Specifying

the model accurately is the most important part of the ana

In circuit analysis programs several different diode m

are used. The built-in model of a diode in NAP2 (Nonlinear Analysis Program) is shown in Figure 3.1.

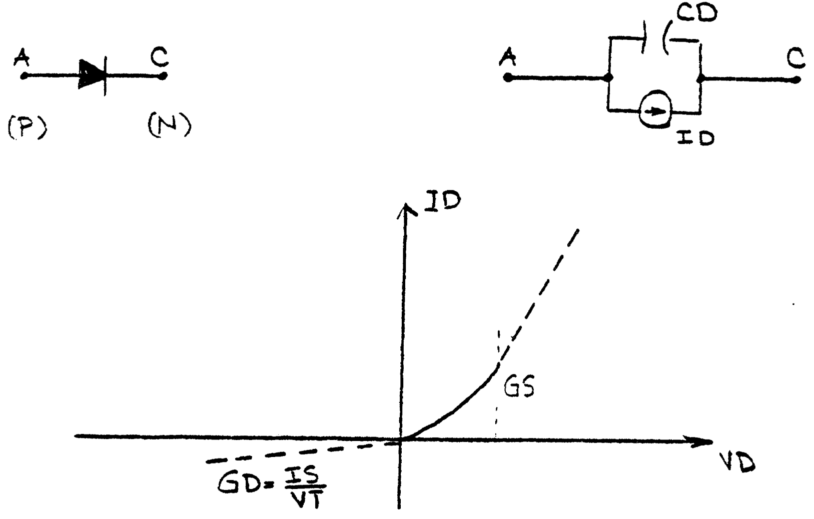


Figure 3.1 NAP2 Built-In Diode Model

NAP2 diode model characteristic is extended linearly when VD< 0, and when the dynamic conductance GD>GS. GS may be specified by the user. The equations for the current ID the charge on capacitor CD, which is QD, are defined in the non-linear region as follows :

$$ID = IS \cdot \left(\exp(VD/VT) - 1 \right)$$

$$QD = \tau_T \cdot ID + \int_0^{VD} CD / \left(1 - (V/\phi)\right)^{\gamma} \cdot dV$$

The variables in the above equation are as follows:

ID: Diode current source

QD: Charge across capacitor CD

IS: Diode reverse saturation current

VD: Voltage across diode

VT: Constant in the capacitor equation of diode

ϕ : Junction potential

Y : Exponent in capacitor equation

T_t : Transition time constant of the diode

CJ: Zero bias junction capacitance

GS: Maximum dynamic conductance

The built-in diode model is referenced in NAP2 circuit descript language as follows:

Txxx Pnode Nnode LISTNAME

LIST NAME is a reference to a previously defined parameter list for the diode:

LIST NAME /DIODE/ IS value VT value TT value CJ value >

FI value GA value GS value

'value[1] can be constant or functional.

Even though the NAP2 diode model has reasonable level of accuracy, there are some disadvantages in using this model. The disadvantages are:

(1) The diode current ID is non-linear only in a small range of the forward biased region. Outside this area linearity is assumed. This model Becomes inadequate when the circuit has failures which may result in high current levels.

(2) The parameter list for the built-in model of dio
is not directly available in the semiconductor data
manuals. The user has to solve lengthy equations usi
the data given in the semiconductor data manuals to o
the parameter list of built-in model.

Because of the above disadvantages and linearization
built-in diode model of NAP2, the SCEPTRE diode model is a
and a corresponding NAP2 model is developed. A large amou
of published SCEPTRE models are available for commonly use
diodes [8].

The SCEPTRE diode model developed in the NAP2 circuit
description language is described below. This model shown
Figure 3.2 is known as the EBERS-MOLL model. The device p
given in SCEPTRE model publication are used in this model

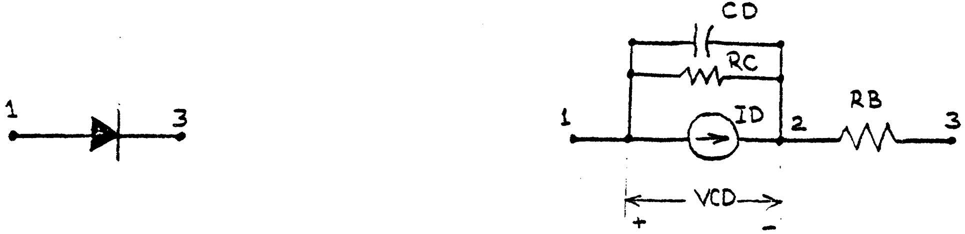


Figure 3.2 SCEPTRE Ebers-Moll Diode Model

The equation of the model are as follows:

$$ID = IS \cdot \left(e^{VCD/VT} - 1\right)$$

$$CD = \frac{CO}{(\phi - VCD)^n} + KD \cdot (ID+IS)$$

CD = The sum of the diode transition and diffusion capacitances

where

$CO/(\phi - VCD)^n$ = Transition capacitance = CJ, and

KD(ID+IS) = Diffusion capacitance

ID = Dependent Current generator representing the diode junctic

current. The generator is a function of voltage VCD,

IS = Diode reverse saturation current

RB = Diode bulk resistance

VT = Co.nstant of the diode equation (volts)

CO = Constant of the transistion capacitance equation

(farads)

ϕ = Junction contact potential (volts)

n = Junction grading constant

KD = Diffusion capacitance constant

= 1 / (VT*2*3.14*F)

F = Frequency parameter

VCD = Voltage across capacitor CD, which is equal to the diode

junction voltage (volts)

The model of the diode model is illustrated for diode IN64

in both SCEPTRE and NAP2 circuit description language. (See Figures 3.3 and 3.4).

```
MODEL 1N645 (PERM).(A-K)
SUPPLIED BY DAVID M. HAR3TAD, SANDIA CORPORATION
SANDIA BASE, ALBUQUERQUE, NEW MEXICO 37115
EBERS-MOLL DIODE MODEL
UNITS-MILLIAMPS-VOLT5-K0HMS-PF-MICROHENRY-NANOSEC
THE VALUES IN THE EQUATION FOR CT CORRESPOND TO THE
PARAMETERS SHOWN 8EL0W :
 1) CO   : CONSTANT OF THE TRANSITION CAPACITANCE EQUATION
 2) <p   : JUNCTION CONTACT POTENTIAL (VOLTS)
 3) VCD  : VOLTAGE ACROSS CAPACITOR CD, WHICH IS
          EQUAL TO THS DIODE JUNCTION VOLTAGE(VOLTS)
 4) N    : JUNCTION GRADING CONSTANT '
 5) KD   : DIFFUSION CAPACITANCE CONSTANT (PFO/MA)
 6) JD   : CURRENT GENERATOR REPRESENTING THE DIODE
         JUNCTION CURRENT.
 7) IS   : DIODE SATURATION CURRENT
THE VALUES Itf THE DIODE EQUATION CORRESPOND
TO THE PARAMETERS BELOW  :
 1) IS   : DIODE SATURATION CURRENT
 2) ©    : CONSTANT OP DIODE EQUATION
ELEMENTS
CT, 1-K = Ql ( 0.103E 02, 0.364E 00, VCT, 0.577E 00,
               0.125E 06, JD, 0.206)
R3, A-l = 0.532E-03
RC, 1-K = 0.123E 09
JD, 1-K = DIODE EQUATION (0.251E-06, 0.261E 02)
FUNCTIONS
01 (A, B, C, D, E, F, G) • ((A/ABSlB-C)**D)+E*{F+G))
```

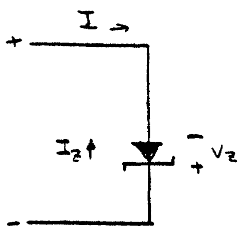
Figure 3.3 SCEPTRE Diode Model for IN645

```
*LIB2 D1N645 +
:internal node 1 is the anode
:internal node 3 is the cathode
CURGEN/EXP/ A -0.25100E-09 B 0.25100E-09 >
               D 0.38314E-01 L -2.00 U 0.10
CDIF / / B 0.12500E-03 C -0.25100E-09
CTRAN / / B 0.10800E-10 C 0.86 D -1 E -0.57700
RS 1 2 0.12300E 09
ID 1 2 1*CURGEN(VID)
CT 1 2 1*CTRAN(VID)
CD 1 2 1*CDIF(IID)
RB 2 3 0.53200E-03
>
```

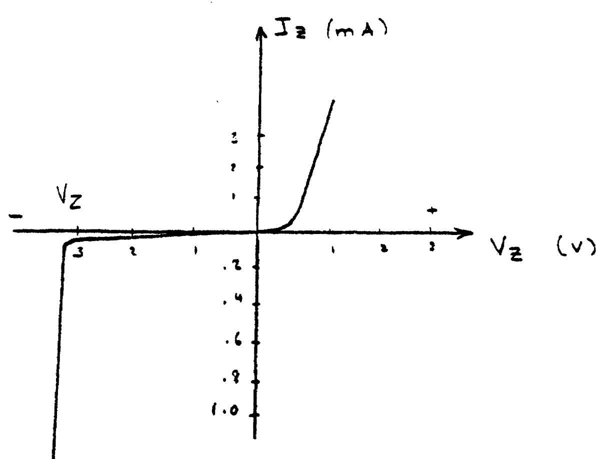
Figure 3.4 NAP2 Diode Model For IN645

B. Zener Diode Model

Typical V-I characteristics of a low voltage reference zener are shown in Figure 3.5. Note that the forward characteristic is similar to that of the regular p-n junction diode.



(a) Breakdown (Zener) diode



(b) Typical V-I characteristics

Figure 3.5 Zener Diode Characteristics

The reverse characteristic shows a breakdown voltage, Vz, which is independent of the diode current. A wide range of zener diodes are commercially available; values from 2 to 200 volts, with power ratings from a fraction of a watt to 100 watts, are common. It should be pointed out, however, that

changes in temperature generally cause a change in the zener reference voltage. The typical temperature coefficient of the zener diode is specified by the manufacturer. For example, the temperature coefficient for zener diode IN752A varies from -1 to 1.5 Mv/°C«

NAP2 does not have a built-in model for the zener diode. The zener diode is modelled by connecting an additional reverse current generator, Iz, parallel to the forward current generator, Id, in the diode model. IZ is defined with a table. The NAP2 zener diode model is shown in Figures 3.6 and 3.

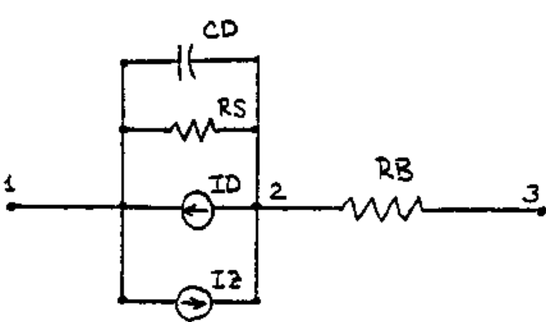


Figure 3.6. Zener Diode Model

```
*LIB2 Z1N752A +
CURGEN/EXP/ A -0.125E-10 B 0.125E-10 >
            D 0.32468E-01 L -2.0 U 0.8
ZENCUR/TAB2/ -3.0 -10.0 >
             -1.0 -6.0 >
             -0.8 -0.5 >
             -0.6 -0.05 >
             -0.5 -0.2E-02 >
             -0.48 -0.1E-08 >
              0.0 0.1E-08 >
              1.0 0.1E-05 >
              4.9 0.1E-05 >
              5.28 0.1E-02 >
              5.34 .02 >
              5.41 .05
CDIF/ / B 0.31E-05 C -0.125E-10
CTRAN/ / B 0.333E-09 C 0.75 >
             D -1.0 E -0.5
RS 1 2 0.1E7
ID 2 1 1*CURGEN(VID)
IZ 1 2 1*ZENCUR(VIZ)
CT 2 1 1*CTRAN(VID)
CD 2 1 1*CDIF(VID)
RB 2 3 11
>
```

Figure 3.7 NAP2 Zener Model For IN752A

C. BIPOLAR JUNCTION TRANSISTOR MODEL

A bipolar junction transistor may be described in terms of two diodes coupled back-to-back. This is not unexpected since a transistor is manufactured by forming two p-n juncti back-to-back. The base region, which is common to both, pro the coupling. The model developed using the above concept i called the EBERS-MOLL model [5]. The built-in model of t bipolar junction transistor used in the NAP2 circuit analysi program is shown in Figure 3.8.

The transistor model in NAP2 is the large signal EBERS- model with non-linear capacitors which represent the charge storage effects of the junctions. The n-p-n model is shown with its characteristic equations.

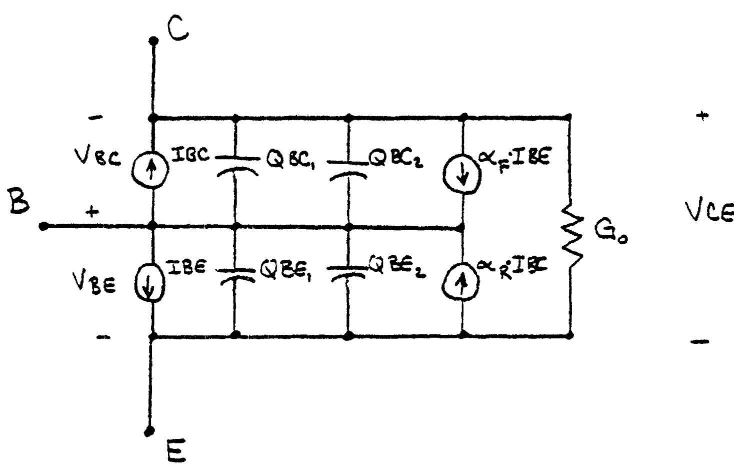


Figure 3.8 NAP2 Built-In Bipolar Junction Transistor Model (NPN)

The equations which govern the BJT model are as follows

$$IBE = IS * (e^{VBE/VT} - 1)$$

$$IBC = NI * IS * (e^{VBC/(NV*VT)} - 1)$$

$$QBE1 = C_{e_j} \int_{o}^{VBE} \frac{dv}{(1-\frac{v}{\phi})^{\gamma}}$$

$$QBE2 = \alpha_F * \tau_F * IBE$$

$$QBC1 = C_{c_j} * \int_{o}^{VBC} \frac{dv}{(1-\frac{V}{\phi})^{\gamma}}$$

$$QBC2 = \alpha_R * \tau_R * IBC$$

The parameters are defined in Table 3.1.

SYMBOL	NAP 2	DESCRIPTION	DEFAULT VALUE
is	IS	Base-Emitter Saturation current	1E-13
VT	VT	Constant in the base emitter diode current equation	0.025
NI	NI	NI*IS is the base collector saturation current	1
NV	NV	NV*VT is the constant in the base-collector diode current equation	1
%	TF	Forward transit time (common base)	0
^	TR	Reverse Transit time (Common Base)	0
Cej	CE	Zero-bias base-emitter caoacitance	0
Ccj	CC	Zero-bias base-col lector-Capacitance	0
*	PI	Junction ootential	1
GA	GA	Exponent in capacitance equation	0.5
6*	GZ	Zero-bias output conductance	0
NG	NG	Proportionality factor for output conductance	0
^	AF	Forward Current Gain (Common Ease)	0.99
^	AR	Reverse Current Gain (Common Base)	0.5
GS	GS	Maximum junction diode conductance	1

Table 3.1 NAP2 BJT Model Parameters

The built-in transistor model is referenced in NAP2 circuit description language as follows:

```
TXXX     Cnode     Bnode     Enode     LISTNAME [AF
```

LIST NAME is a reference to a previously defined paramet list for the transistor :

```
LISTNAME /  / AF value AR value IS value NI value >
 VT value NV value TF value TR value GE value >
 CC value FI value GA value GZ value NG value >
 GS value
```

'Value' can be constant or functional. The curr AF can be specified as a parameter in the transistor ref statement.

The NAP2 BJT model has some disadvantages. They ar

(1) The diode current sources IBE and ICE are non- only in certain areas of the forward biased region. this area linearity is assumed. This model becomes inadequate when the circuit has failures.

(2) Some of the parameters like ϕ are assumed to b for C-B and B-E junctions.

(3) Bulk resistances of transistors can only be re as external resistances to the model.

(4) Finally, the parameter list for the built-in m of BJT is not directly available in the transistor So, the user has to solve complicated equations usi data given in transistor manuals to match the param list of the built-in model.

Because of the above disadvantages and short comings of the built-in transistor model of NAP2, the SCEPTRE model is adopted for use in the NAP2 circuit analysis program. The SCEPTRE model library contains a large number of commonly used transistor models. The SCEPTRE model is shown in Figure 3.9.

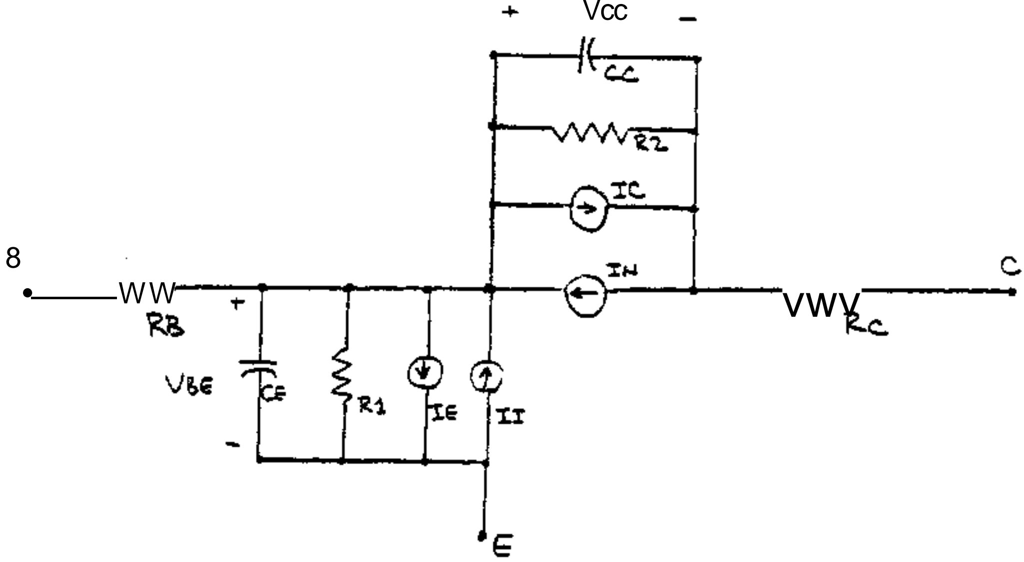


Figure 3.9 SCEPTRE Bipolar Junction Transistor

The equations which govern the SCEPTRE model are as follows:

$$CE = \frac{COE}{(\Phi_E - VCE)^{n_E}} + (TE/VTE)\cdot(IE + IES)$$

$$CC = \frac{COC}{(\Phi_C - VCC)^{n_C}} + (TS/VTC)\cdot(IC + ICS)$$

$$\cdot\left(e^{VCE/VTE} - 1\right)$$

$$IC = ICS \cdot \left(e^{VCC/VTC} - 1\right)$$

$$IN = \alpha_F \cdot IE$$

$$II = \alpha_R \cdot IC$$

$$\alpha_F = F1(IE)$$

$$\alpha_R = F2(IC)$$

base junction

η_e = Emitter junction grading constant

η_c = Collector junction grading constant

IN « cunent generator dependent on the emitter base junction current

II = current generator dependent on the collector base junction current.

IES » Emitter base saturation current measured in the active region

ICS » collector base saturation current measured in the active region

VTE = constant of the emitter base junction eauation

VTC « constant of the collecor base junction eauation

TE » Time constant of the emitter diffusion capacitance eauation

= (1 / (2 * 3*14 * FF))

TS = Time constant of the collector diffusion capacitance equation

« (1 / (2 * 3.14 * PR.))

FF a The average fT normal

FR.a The average fT inverse

^p a Forward current gain

This parameter is entered as a function of IE in the SCEPTRE model

R3 a Hase bulk resistance

RC a Collector bulk resistance

Rl a Emitter base junction leakage resistance

$TE = F3 (IE)$

$TS = F4 (IC)$

DEFINITION OF PARAMETERS.

CE = The sum of the emitter transition and diffusion capacitances, where:

$\{ COE / (\phi_E - VCE)^{n_E} \}$ = emitter transition capacitance

and

$\{ TE/VTE \} \cdot \{ IE+IES \}$ = emitter diffusion capacitance

CC = The sum of the collector transition and diffusion capacitances, where

$\{ COC / (\phi_c - VCC)^{n_c} \}$ = collector transition

$\{ TS / VTC \} \cdot \{ IC+ICS \}$ = collector diffusion

COE = constant of the emitter transition capacitance equation

COC = Constant of the collector transition capacitance equation

ϕ_E = Emitter base junction contact potential

ϕ_c = Collector base junction contact potential

IE = current generator representing the emitter base junction

IC = current generator representing the collector

R2 = collector base junction leakage resistance

The description given above was for NPN transistor model. A PNP transistor is modelled by reversing the polarities of th current sources in the NPN model. Figures 3.10 and 3.11 depicit the SCEPTRE and NAP2 statements which model transistor 2N329A.

```
MODEL 2N329A (PERM) (B-C-E)
SUPPLIED BY CONVAIR DIVISION, GENERAL DYNAMICS,
              SAN DIEGO CALIF.92112
UNITS OHMS,VOLTS,AMPS,FARADS,HENRIRS,SECONDS
ELEMENTS
RQ, 1-E = 350.0
RC, C-2 = 32.0
RE, E-3 = 2.5
RCC,2-1 = 5.0E 07
REE,3-1 = 5.0E 07
CE, 3-1 = EQUATION1 (2P.OE-12,.SO,VC£,.47,39.,8.8E-08,
                        JE,2.16E-14)
CC, 2-1 = EQUATION1 (95.E-12,.80,VCC,.50,29.,1.4E-05,
                        JC,6.22E-11)
JE, 3-1 = DIODE EQUATIOW (2.16E-14, 39.)
JC, 2-1 = DIODE EQUATION (6.22E-11,29.)
JI, 1-3 = 0.865*JC
JN, 1-2 = 0.972*JE
JPl,l-3 = 0.
JP2,l-2 • 0.
FUNCTIONS
EQUATION! (A, B, C, D, E, F, G, H) = (A/(B-C)**D+E*F*(G+H))
```

Figure 3.10 SCEPTRE Model For Transistor 2N329A

```
*LIB2 TR2N329A +
: INTERNAL NODE 1 IS COLLECTOR
: INTERNAL NODE 2 IS BASE
: INTERNAL NODE 3 IS EMITTER
EMTRAN/ / B 0.28000E-10 C 0.8 D -1 E -0.47000
:EMTRAN.B IS CONSTANT OF THE EMITTER TRANSITION >
CAPACITANCE (COE)
:EMTRAN.C IS EMITTER BASE JUNCTION CONTACTPOTENTIAL (FIE)
:EMTRAN.D IS -1
:EMTRAN.E IS NEGATIVE OF EMITTER JUNCTION GRADING >
CONSTANT (-NE)
EMTCUR/EXP/ A -0.216E-13 B 0.216E-13 D 0.25641E-01 >
              L -8.0 U 0.7
:EMTCUR.B IS EMITTER BASE SATURATION  CURRENT MEASURED IN >
                         THE ACTIVE REGION
:EMTCUR.D IS THE INVERSE OF CONSTANT OF EMITTER >
BASE JUNCTION EQUATION (VTE)
EMTDIF/ / A 0.21600E-13
COLDIF/ / A 0.62200E-10
COLLCUR/EXP/ A -0.622E-10 B 0.622E-10 >
             D 0.34482E-01 L -8.0 U 0.7
:COLLCUR.A IS NEGATIVE OF COLLECTOR BASE SATURATION >
 CURRENT MEASURED IN THE ACTIVE REGION
:COLLCUR.B IS THE COLLECTOR BASE SATURATION CURRENT >
               MEASURED IN THE ACTIVE REGION
:COLLCUR.D IS THE INVERSE OF CONSTANT OF COLLECTOR >
 BASE JUNCTION EQUATION (VTC)
CLTRAN/ / B 0.96000E-10 C 0.80000E+00 D -1 E -0.50000E+00
:CLTRAN.B IS CONSTANT OF THE COLLECTOR >
 TRANSITION CAPACITANCE EQUATION (COC)
:CLTRAN.C IS COLLECTOR BASE JUNCTION CONTACT >
 POTENTIAL (FIC)
:CLTRAN.D IS -1
:CLTRAN.E IS NEGATIVE OF COLLECTOR JUNCTION >
  GRADING CONSTANT (-NC)
RB 2 4 350.00000 :BASE BULK RESISTANCE
R1 4 3 0.50000E+08 :EMITTER BASE JUNCTION >
                              LEAKAGE RESISTANCE
IE 3 4 1*EMTCUR(VIE)
CET 4 3 1*EMTRAN(VIE)
PTEMP6=0.88E-07
PTEMP1= 0.39E+02*PTEMP6
PTEMP2 = 1* EMTDIF(IIE)
CED 4 3 1*PTEMP1*PTEMP2
IN 4 5 0.97200E+00 IIE
R2 4 5 0.50000E+08 :COLLECTOR BASE JUNCTION >
                              LEAKAGE RESISTANCE
```

```
IC 5 4 1*COLLCUR(VIC)
CCT 4 5 1*CLTRAN(VIC)
PTEMP7=0.14E-04
PTEMP3 = 0.29001E+02*PTEMP7
PTEMP4 = 1*COLDIF(IIC)
CCD 4 5 1*PTEMP3*PTEMP4
II 4 3 0.86600E+00 IIC
RC 5 1 0.32000E+02 :COLLECTOR BULK RESISTANCE
>
```

Figure 3.11 NAP2 Model For Transistor 2N329A

3.2 NOMINAL COMPONENT AND FAILURE MODELLING

The analysis of a circuit when all of its components have nearly the nominal value yields the nominal response. Typically circuit components have 1%, 5% or 10% tolerance specified on their nominal values. The actual value of a 1 kohm resistor in a circuit having 5% tolerance resistors may be any resistance between 950 and 1050 ohms. In the circuit analysis all componen tolerances are taken into consideration in the computation of the approximate worst case response. The sign of the sensitivit of the desired response with respect to the nominal component value (or parameter) indicates if the minimum or maximum value of the component value should be used to compute the worst case response. To compute the minimum worst case response, minimum component value is used when the sign of the sensitivity is positive. However if the sign is negative, maximum component value is used. To compute the maximum worst case response, maximum value is used when the sign of the sensitivity is positi If the sign is negative, minimum component value is used. With these values two additional simulations are performed to get an estimate of the minimum and maximum worst case response.

If a tolerance is not specified, circuit simulation uses the same value when computing the nominal, minimum and maximum worst case responses. This is a very unlikely physical situatio

NOPAL Resistance Measurement Function Used in a Conjunction

<CNX_H1, CNX_LO > = OHMMETER(RES,MIN,MAX,VREF)

where

'OHMMETER.CNX01' ← high test point CNX_H1

'OHMETER.CNX02' ← low test point CNX_LO

'OHMMETER.PRM01' ← measured resistance RES

'OHMMETER.PRM02' ← minimum resistance MIN

'OHMMETER.PRM03' ← maximum resistance MAX

'OHMMETER.PRM04' ← reference voltage VREF

Figure 3.15 NOPAL Ohmmeter as ATLAS Procedures

Table 3.2 illustrates the typical tolerances used in NOPAL:

Component Type	Tolerance Value (+, −)	Tolerance on Paramet
Resistor	10%	Resistance
Capacitor	10%	Capacitance
Inductor	10%	Inductance
Diode (and Zeners)	5%	Reverse Saturation
Transistor (BJT)	0.5%	Forward and Revers
		Alpha When α < 0.995

Table 3.2 Component Tolerances

A 10% tolerance indicated in the table represents -10% and +10% of the nominal value. If so required different negative and positive tolerances can be specified. When the circuit schematics don't specify otherwise, the tolerance shown above are used. The tolerances on transistor reverse and forward alphas should be carefully specified to ensure that the maximum value of alpha is less than one. Even though it is theoreticall possible to have negative resistances in circuit designs, -200% tolerance on a 20 ohm resistance (implies -20 ohm) is obviously, an errorneous specification.

In the NOPAL system most single component failures are modelled by topological changes in the circuit description. Eve though in this study only single catastrophic failures (open anc short) are investigated, any other failure (i.e. multiple) can 1: modelled using any combination of single failures and out-of-

tolerance parameters.

Single catastrophic failures which are automatically genera
by the NOPAL system (whenever applicable to a component in the circuit) are tabulated and pictorially explained in Figure 3.12 All resistor, potentiometer, capacitor diode and zener diode failures are modelled with a resistance replacing the component. Transistor failures are essentially the same as the others with an additional low valued resistor shorting the junction which is open. This model of junction-open failure prevents numerical analysis and modelling problems associated with the Ebers-Moll model of bipolar-junction transistor.

3.3 Stimulus and Measurement Device Modelling

Each range of the stimulus and measurement devices of an ATE result different loading conditions to a unit under test. These loading effects and signals must be effectively modelled and simulated accurately. Especially the behavior of the non-linear circuit components is critically dependent on the stimulu and measurement devices. In the following subsections, resistar impedance, voltage and current measurement models and power supply models are described.

A. Resistance Measurement

EQUATE performs resistance measurements by setting up a dc-standard reference voltage, a standard resistance in series with the unknown resistance connected through the PIU/DIU test

Component	Failure Function	Pictorial	Nominal	Minimum (in ohms)
Resistor	Open		10 Meg	1 Meg
	Short		1	0.1
Capacitor	Open		10 Meg	1 Meg
	Short		1	0.1
Diode/Zener	Open		10 Meg	1 Meg
	Short		1	0.1
Transistor	Collector Open	Rshort Ropen	R short :	same as re
	Base Open	Ropen	R open:	same as re
	Emitter Open	Rshort Ropen		
	Base-Collector Short	Rshort		
	Base-Emitter Short	Rshort		
	Emitter-Collector Short	Rshort		

Figure 3.12 Single Catastrophic Failure Models in NOPAL

points. A voltmeter measures the voltage drop across the unknown resistance. This measured voltage is used with the other user provided data to compute the unknown resistance in software (Figure 3.13).

The ohmmeter setup described above is also modelled for NAP2 to make resistance measurements. In the NAP2 circuit analysis program it is more convenient to work with branch currents; hence in the circuit simulation the current through the reference voltage is requested and a slightly different equation is used to compute R_x (Figure 3.14).

The ATLAS resistance measurement procedure used by the NOPAL system is shown in Figure 3.15. In this procedure the range is selected according to the minimum expected resistanc However if the measurement is higher than the upper limit of the selected range (overrange) and maximum expected resistanc is greater than the measured value, then the measurement is repeated in the next higher range. To eliminate the effects charging and discharging time of capacitors dc standard is applied and measurements are repeated until the relative errc in two successive measurements is less than or equal to 0.1%. However this accuracy is not enfored when the measurement is greater than lOMohm. This is the highest resistance that can measured by the equipment.

B. Impedance Measurement

The impedance measurement operation in the EQUATE is sin to resistance measurement. Figure 3.16 depicts the setup used in impedance measurements. The impedance is computed fi

ATLAS Statement To Measure Resistance:

MEASURE (RES 'RX' OHM),IMPEDANCE, RES MAX 'RES MAX 'RMAX' OHM

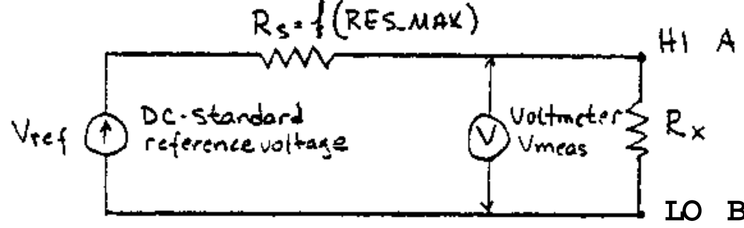
REF-VOLTAGE 'VREF' V, DELAY 'D' SEC,

CNX HI 'A' LO 'IS' $

Where the control limitations are:

FIELD	RANGE;
RES MAX	0 to 10 Mohm
REF-VOLTAGE	-10 to +100 SEC

Circuit Equivalent Equipment Setup:



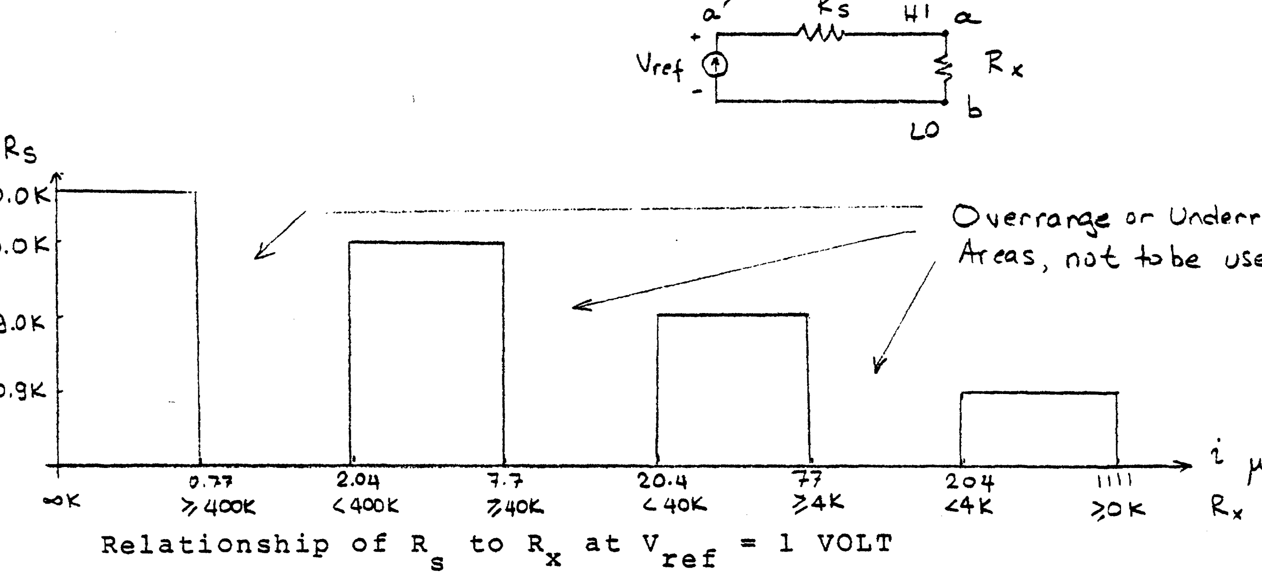
Series resistance of R_s is programmed by the system depending on the RES MAX field as follows:

R_s	RES_MAX
0.9 Kohm	$0 \leq R_{max} < 4$ Kohm
9.0 Kohm	$4 \leq R_{max} < 40$ Kohm
90.0 Kohm	40 Kohm $\leq R_{max} <$ 400 Kohm
900.0 Kohm	400 Kohm $\leq R_{max}$

The voltage drop across R_x is measured by the voltmeter 'D' seconds after the dc-standard voltage source is applied. The foil equation is used to compute the unknown resistance:

$$R_x = \frac{V_{meas} \times R_s}{V_{ref} - V_{meas}}$$

Figure 3,13 EQUATE Resistance Measurement



Relationship of R_s to R_x at V_{ref} = 1 VOLT

To obtain the current levels at V_{ref} other than 1volt, multiply 'z' by the desired V_{ref}. Above ohmmeter written in NAP2 language is:

```
:
FRANGE/TAB2/  0        900K     0.77U     900K       >
              0.77U     90K      2.04U     90K       7.7U 90K >
              7.7U       9K     20.40U      9K       77 U  9K >
              77U      0.9K      204U     0.9K        1   0.9K
RVREF  b   a'   0   E  Vref
RS     a'  a     1*FRANGE(IRS)
*DC  *WORST     IROHMTR
:
```

Unknown resistance is computed using:

$$R_x = \frac{V_{ref} * R_s(i)}{i}$$

Figure 3.14 NOPAL Model of the EQUATE Ohmmeter for NAP2

```
EFINE  PROCEDURE, 'OHMMETER'$
  DECLARE DECIMAL, 'OHMMETER.PRMO1',
        'OHMMETER.PRMO2','OHMMETER.PRMO3','OHMMETER.PRMO4',
        'OHMMETER.RES','OHMMETER.MAX','OHMMETER.LL','OHMMETER.UL',
        'OHMMETER.LAST','OHMMETER.COUNT','OHMMETER.LRI','OHMMETER.URI'
        'OHMMETER.CNXO1','OHMMETER.CNXO2'$
 DECLARE DECIMAL, LIST, 'OHMMETER.RNG'(5) $
'OHMMETER.RNG'(1) = 0 $
'OHMMETER.RNG'(2) = 3999   $  'OHMMETER.RNG'(3) = 39999 $
'OHMMETER.RNG'(4) = 399999 $  'OHMMETER.RNG'(5) =  1E6 $
'OHMMETER.LAST' = -1 $
'OHMMETER.COUNT' = 0 $
 COMPARE 'OHMMETER.PRMO2', LT 4000 $  GOTO STEP  11 IF NOGO $
        'OHMMETER.LRI' = 2 $ GOTO STEP 14 $
 COMPARE 'OHMMETER.PRMO2', LT 40000 $  GOTO STEP 12 IF NOGO $
        'OHMMETER.LRI' = 3 $ GOTO STEP 14 $
 COMPARE 'OHMMETER.PRMO2', LT 400000 $  GOTO STEP 13 IF NOGO $
        'OHMMETER.LRI' = 4 $ GOTO STEP 14 $
        'OHMMETER.LRI' = 5 $
 COMPARE 'OHMMETER.PRMO3', LT 4000 $  GOTO STEP  15 IF NOGO $
        'OHMMETER.URI' = 2 $ GOTO STEP 18 $
 COMPARE 'OHMMETER.PRMO3', LT 40000 $  GOTO STEP 16 IF NOGO $
        'OHMMETER.URI' = 3 $ GOTO STEP 18 $
 COMPARE 'OHMMETER.PRMO3', LT 400000 $  GOTO STEP 17 IF NOGO $
        'OHMMETER.URI' = 4 $ GOTO STEP 18 $
        'OHMMETER.URI' = 5 $
 'OHMMETER.MAX' = 'OHMMETER.RNG'('OHMMETER.LRI') $
  COMPARE 'OHMMETER.CNXO1' + 'OHMMETER.CNXO2', LE 200 $
     GOTO STEP 19 IF GO $
     DISPLAY "PROBE HI ", 'OHMMETER.CNXO1', "[illegible] LO ", 'OHMMETER.CNX(
  MONITOR (RES 'OHMMETER.PRMO1' OHM),IMPEDANCE,
        REF-VOLTAGE 'OHMMETER.PRMO4' MV, RES MAX 'OHMMETER.MAX' OHM,
        CNX PROBE $
  'OHMMETER.COUNT' = 1 $
  GOTO STEP 21 $
  INITIATE (RES 'OHMMETER.PRMO1' OHM),IMPEDANCE,
        REF-VOLTAGE 'OHMMETER.PRMO4' MV, RES MAX 'OHMMETER.MAX' OHM,
        CNX HI 'OHMMETER.CNXO1' LO 'OHMMETER.CNXO2'$
 READ (RES 'OHMMETER.PRMO1' OHM), IMPEDANCE $
'OHMMETER.COUNT' = 'OHMMETER.COUNT' + 1 $
 COMPARE 'OHMMETER.PRMO1', GT 1OE6$ GOTO STEP 21 IF GO $
 COMPARE ABS(('OHMMETER.PRMO1'-'OHMMETER.LAST')/'OHMMETER.PRMO1'), LE
'OHMMETER.LAST'='OHMMETER.PRMO1'$  GOTO STEP 20 IF NOGO$
 RECORD 'AFF-COMP.TEST',"TEST [illegible] ",'OHMMETER.PRMO1'/1E3,
   "[illegible] KOHM, ",'OHMMETER.PRMO4'," [illegible] MV, ",
  ('OHMMETER.MAX'+1)/1E3, "[illegible] KOHM, ",'OHMMETER.COUNT'," [illegible] TIMES,
   "CNX(",'OHMMETER.CNXO1',"[illegible],",'OHMMETER.CNXO2',"[illegible])"$
 COMPARE 'OHMMETER.PRMO1',
        UL 'OHMMETER.RNG'('OHMMETER.LRI') $  GOTO STEP 22 IF GO $
'OHMMETER.LRI' = 'OHMMETER.LRI' +1 $
 COMPARE 'OHMMETER.LRI', GT 'OHMMETER.URI' + 0.5 $ GOTO STEP 18 IF NO
 REMOVE DC-STD $
 END 'OHMMETER'$
*************************************************************************$
```

Figure 3.15 (continued) NOPAL Ohmmeter as ATLAS Procedure

the measured voltage across the unknown load. A reference voltage from the ac-standard is applied through a scaling resisto to the unknown. The frequency and voltage setting of the ac standard are programmable. R_s is a series resistance whose value is determined by the system depending on the maximum expected impedance. R_m and C_m are the parallel RC network which represent the sampler impedance. Z_x is the unknown impedance to be measure Z_x is computed from the Z_{total} after compensating for Z_m. Z_{total} is computed from the voltage measurement taken across Z_x. It has been determined that the programming data given for the impedance measurement are not attainable identically on EQUATEs V and VII. The compensation used (R_m = 1Mohm and C_m = 900pF) is not adequate. EQUATE V fails to make impedance measurements abov 8KHz. However EQUATE VII can measure up to 12KHZ.

The model of the impedance measurement function as used by the NOPAL system in NAP2 language is shown in Figure 3.17.

The ATLAS impedance measurement procedure used by the NOPAL system is shown in Figure 3.18. In this procedure the range is selected according to the minimum expected impedance. However if the measurement is higher than the upper limit of the selected range (overrange) and maximum expected resistance is greater than the measured value, then the measurement is repeated in the next higher range. To eliminate the effects of settling times and ac-standard setup time at each different frequency, the measurements are repeated until the relative error in two successive measurements is less than or equal to 0.1%. This accuracy is not enforced if the measurement is greater than 10 Mohm.

ATLAS Statement to Measure Impedance:

```
MEASURE(IMP 'ZX'(1)OHM),IMPEDANCE, IMPMAX 'ZMAX'OHM,
     FREQ 'ZF' HZ, REF-VOLTAGE 'ZEIN',
     DELAY 'D' SEC, CNX HI 'A' LO 'B' $
```

FIELD	USER MANUAL RANGE	PROGRAM RANGE
IMP MAX	0-10 Kohm	0-10 Mohm
FREQ	10HZ-7KHZ	10HZ-12.5KH!
REF-VOLTAGE	0-7 Vrms	0-7 Vrms
DELAY	1 msec-100 sec	lmsec-100se<

Circuit Equivalent Equipment Setup:

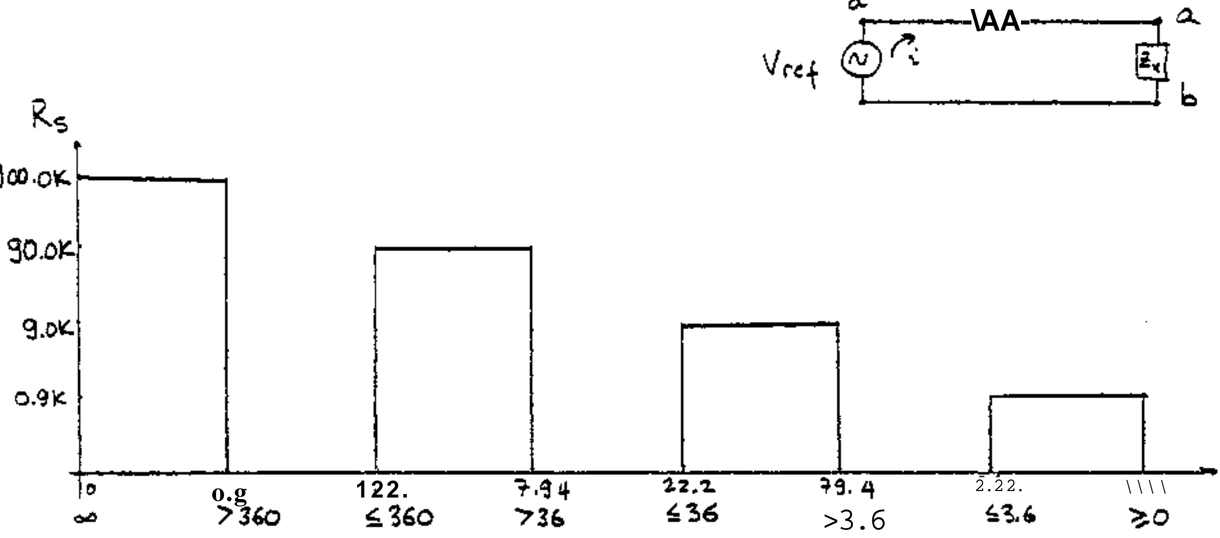
Rs is programmed by the system depending on IMP MAX field as follows:

Rs	Imp MAX
0.9 Kohm	$0 \leq Z_{max} \leq 3.6$ Kohm
9.0 Kohm	3.6 Kohm ≤ 36 Kohm
90.0 Kohm	36 Kohm < Z_{mos} ≤ 360 Kohm
900.0 Kohm	360 Kohm < Z_{max}

The sample makes eight measurements for period of the reference frequency. The Fourier transform is taken to get th real and imaginary parts of the fundamental component. The following equation is used to compute the complex impendance.

$$\frac{1}{Z_x} = \frac{\frac{E_{in}}{E_{out}} - 1}{R_s} - \frac{1}{Z_m}$$

Fiaure 3.16 EOTTATK Impedance Measurement



Relationship of R_s to Z_x at V_{ref} = 1 Volt rms.

To obtain the current levels at other than V_{ref} = IV multipl by the disired V_{ref}. This impedance measurement is wri in NAP2 as follows:

```
FRANGE/TAB2/ 0      900K     0.8y     900K    >
             0.8y   90K      2.22y    90K     7.94y   90K    >
             7.94y  9K       22.2y    9K      79.4y   9K     >
             79.4µ  0.9K     222y     0.9K    I       0.9K
ZESRC        b      a'       O   E    vref
RS           a'     a        1*  FRANGE(IRS)
*DC;*RUN
*AC  *PRINT  *MA  *PH  IPS
```

The simulation gives the magnitude (i) and phase θ) of the current through Rs.

The impedance seen by the meter is:

$$Z_x = \frac{V_{ref} - R_s * i \angle\theta}{i \angle\theta}$$

magnitude of $Z_x = ((V_{ref} - R_s * i * \cos\theta)^2 + (R_s * i * \sin\theta)^2)^{\frac{1}{2}}$

phase angle $= \arctan\left(\frac{R_s * i * \sin\theta}{V_{ref} - R_s * i * \cos\theta}\right) - \theta$

Figure 3.17 NOPAL Model of EQUATE Impedance Meter for NAP2

NOPAL Impedance Measurement Function Used in a Conjunction

<CNX_H1, CNX_LO> =ZMETER(IMP,MAX,VREF,FREQ)

'ZMETER_CNX01'	=	high test point	CNX_H1
'ZMETER.CNX02'	=	low test point	CNX_LO
'ZMETER.PRM01'	=	measured impedance	IMP
'ZMETER.PRM02'	=	minimum impedance	MIN
'ZMETER.PRM03'	=	maximum impedance	MAX
'ZMETER.PRM04'	=	reference voltage	VREF
'ZMETER.PRM05'	=	frequency	FREQ

Figure 3.18 NOPAL Impedance Meter as ATLAS Procedure

```
DEFINE PROCEDURE, 'ZMETER'$
   DECLARE DECIMAL, 'ZMETER.PRMC1',
        'ZMETER.PRMC2','ZMETER.PRMC3','ZMETER.PRMC4','ZMETER.PRMC5',
        'ZMETER.RES','ZMETER.MAX','ZMETER.LL','ZMETER.UL',
        'ZMETER.LAST','ZMETER.COUNT','ZMETER.LRI','ZMETER.URI',
        'ZMETER.CNXC1','ZMETER.CNXC2'$
   DECLARE DECIMAL, LIST, 'ZMETER.ARG'(3),'ZMETER.RNG'(5) $
  'ZMETER.RNG'(1) = 0 $
  'ZMETER.RNG'(2) = 3E00    $  'ZMETER.RNG'(3) = 3E000 $
  'ZMETER.RNG'(4) = 3E0000 $  'ZMETER.RNG'(5) =  1E6 $
  'ZMETER.LAST' = -1 $
30 'ZMETER.COUNT' = 0 $
   COMPARE 'ZMETER.PRMC2', LE 3E00 $  GOTO STEP  31 IF NOGO $
        'ZMETER.LRI' = 2 $ GOTO STEP 34 $
31  COMPARE 'ZMETER.PRMC2', LE 3E000 $  GOTO STEP 32 IF NOGO $
        'ZMETER.LRI' = 3 $ GOTO STEP 34 $
32  COMPARE 'ZMETER.PRMC2', LE 3E0000 $  GOTO STEP 33 IF NOGO $
        'ZMETER.LRI' = 4 $ GOTO STEP 34 $
33      'ZMETER.LRI' = 5 $
34  COMPARE 'ZMETER.PRMC3', LE 3E00 $  GOTO STEP  35 IF NOGO $
        'ZMETER.URI' = 2 $ GOTO STEP 38 $
35  COMPARE 'ZMETER.PRMC3', LE 3E000 $  GOTO STEP 36 IF NOGO $
        'ZMETER.URI' = 3 $ GOTO STEP 38 $
36  COMPARE 'ZMETER.PRMC3', LE 3E0000 $  GOTO STEP 37 IF NOGO $
        'ZMETER.URI' = 4 $ GOTO STEP 38 $
37      'ZMETER.URI' = 5 $
38 'ZMETER.MAX' = 'ZMETER.RNG'('ZMETER.LRI') $
   COMPARE 'ZMETER.CNXC1' + 'ZMETER.CNXC2', LE 200 $
     GOTO STEP 39 IF GO $
     RECORD "PROCS HI ", 'ZMETER.CNXC1', "*** LO ", 'ZMETER.CNXC2',"***
  MONITOR (IMP 'ZMETER.ARG'(1) OHM-DEG-HZ),IMPEDANCE,  FREQ 'ZMETER.PRM
        REF-VOLTAGE 'ZMETER.PRMC4' MV, RES MAX 'ZMETER.MAX' OHM,
        CNX HI 'ZMETER.CNXC1' LO 'ZMETER.CNXC2'$
  'ZMETER.COUNT' = 1 $
   GOTO STEP 41 $
39  INITIATE (IMP 'ZMETER.ARG'(1) OHM-DEG-HZ),IMPEDANCE,  FREQ 'ZMETER.P
        REF-VOLTAGE 'ZMETER.PRMC4' MV, RES MAX 'ZMETER.MAX' OHM,
        CNX HI 'ZMETER.CNXC1' LO 'ZMETER.CNXC2'$
40  READ (IMP 'ZMETER.ARG'(1) OHM-DEG-HZ), IMPEDANCE$
   'ZMETER.PRMC1' = 'ZMETER.ARG'(1) $
   'ZMETER.COUNT' = 'ZMETER.COUNT' + 1 $
   COMPARE 'ZMETER.PRMC1', GT 10E6$ GOTO STEP 41 IF GO $
   COMPARE ABS(('ZMETER.PRMC1'-'ZMETER.LAST')/'ZMETER.PRMC1'), LE 1E-3$
  'ZMETER.LAST'='ZMETER.PRMC1'$  GOTO STEP 40 IF NOGO$
41  RECORD 'APP-COMP.TEST',"TEST ::: ",'ZMETER.PRMC1'/1E3,
      "**** KOHM","",'ZMETER.ARG'(2),"*** DEG. ",
      'ZMETER.ARG'(3),"*** HZ, ",'ZMETER.PRMC4',"**** MV, ",
      ('ZMETER.MAX')/1E3, "**** KOHM, ",'ZMETER.COUNT'," :: TIMES, ",
      "CNX(",'ZMETER.CNXC1',"*-,",'ZMETER.CNXC2',"**)"$
   COMPARE 'ZMETER.PRMC1',
          UL 'ZMETER.RNG'('ZMETER.LRI') $  GOTO STEP 42 IF GO $
  'ZMETER.LRI' = 'ZMETER.LRI' +1 $
   COMPARE 'ZMETER.LRI', GT 'ZMETER.URI' + 0.5 $ GOTO STEP 39 IF NOGO $
42  REMOVE AC-STD $
   END 'ZMETER' $
```

Figure 3.18 (continued) NOPAL Impedance Measurement as ATLAS Procedure

VOLTMETER, AMPMETER AND POWER SUPPLIES

The Stimulus functions which apply the power supplies and the
asurement functions which take voltage and current measurements
e simpler than the resistance and impedance measurements. In
is particular application the internal resistance and loading effe
the stimulus and measurement devices could be ignored. This
mplifies the task significantly because the circuit analysis pro-
am can provide the voltage and current measurements directly. The
fferent power supply requirements can be handled by writing a
fferent function for each power supply available on the EQUATE.
gure 3.19 shows the most common power supply and measurement
nctions used in the test specifications.

```
( I * * * * * * * * * * * * * * * * * * * * * * * * * * *   * > « V * x * * * A *   * * * * * * * * * * * * * * * * * * * > * * * * * * * * *
   DEFINE   PROCEDURE,'VOLTMETER' $
DECLARE DECIMAL,'VOLTMETER.PRMC1','VOLTMETER.RES',
                    'V0LTMEIEh•CNXCI"/vOI r-cT:K•C*<X;?u."?•
      ^~A SURE   (VOiTnbL 'VGLTMETc'=?•SfcS" v),
                DC-SIL^ALi DELAY  'j .1   SEC %
                C»V<   HI   'VOLT'c'cTcH.C^Xu1'
                LG   'VOLT^j£T£R.C^X C2"   X
?C        MEA5Uh't   (VOLTAGE  'V OL Tr STcP.F h~.u1"   V),
^                 DI-SIv.J,AL,O£LAY  J»1   S'tC,
                CNX   HI   "VOLTfETwR#cN;XG1'
                LO   ^VCir^ETcK. CNX J<:^   i
  COMPARE ('VOLTMETER.PRMC1'-'VOLTMETER.RES'/'VOLTMETER.PRMC1',
               L£   C.."u'^
  GoTO  STtP  7C  IF  NOGO^
RECORD  'AFF-COMP.TEST',"TEST  ..: MEASURED ".'VOLTMETER.PRMC1',
          ••i.T^.-='   V,   Cr*X   HI   %
          'VOLT:'":T^.CNX01',"•   LO ' >4 t "VOLTi'S T-R?C\'X02*,'':^   ."   ^
  END  'VOLTMETER'  *
C*************************************************************************
  D£F:\t    PROCEuU^E,"ESUPHLr^  $
DELLA •"£  L) EL If. ALf "-'^L'P.DLY.^S^G1', 'E^Ufr-PLY•PRf'D?',^E SUPPLY•REs',
      "rl SUPPLY. CuVu*r',   'LSUPPLY•CNXCi "^
REMOVE   DC2Ai
APPLY  OC-SiGUfIL  DCZA.VOLTAbE   *&SuPrLt•PRrtC1'  Vt
          CNX   HI   'EtUPTLY.Cr*X.;i #   L^   *iSuP FLY.C -'A JZ*   %
RECORD  'AfF-CCf'^.T£ST%"TEST  -* :  AFPLIcD  DC?A',  M,
          "cSUPPLY.P-.VJi"f u -•.  ~  •-"-  ^Jj   C<>A'   HI   M.
          'SSUPPLY. C*:XC1',"•:   LC   ",
          'tSUPPLY.C'ACZ',*1^   ."   i
   MEASURE  (CURRENT  *iSUPFLY.KE3*   A)f
     OC-SlGUAutDEL^Y  0.1  £EC,CNX  OCcA  1
    ^eCORD  "          hEASLR'30 "f *cS'uPl-LY•n*S^y     "'•-*-  -  AMPS  T
  END  'cSUPPLY'  1   .
C*************************************************************************
```

Figure 3«19 NOPAL Stimulus and Measurement Functions as ATLAS Procedures

3.4 ATE-UUT INTERCONNECTING DEVICE

A2100 and A5100 circuit cards are connected to the E
through a custom made interconnecting device (ICD) manufa
by RCA. This ICD has only a few passive elements and prov
the proper sockets and edge connections to route the ATE a
signals to the appropriate pins. The circuit components f
the ICD are the leak resistors which discharge the capacit
the attached UUT after the stimulus has been removed. The
extra resistors are treated as a part of the UUT in circui
simulation. The ICD is intended for use with only one cir
card at a time.

Figure 3.20 is the interface schematic when A2100 car
is being tested. The ICD box is attached to the EQUATE th
cable CA1. Similarly Figure 3.21 is the interface schemat
when A5100 card is inserted. In addition to cable CA1, ca
is attached to provide the lines to the three different po
supplies which are used in testing A5100.

In addition to the resistors, the ICD box contains a
capacitors. However these capacitors are not involved in
tests of A2100 and A5100. The ICD has several other slots
inserting other cards from the AN/VRC12 radio. Figure 3.2
illustrates the hookup of the ICD to the EQUATE.

ATE FUNCTION	TP	J	PIN	P	CABLE CA1	P	PIN	J	7«47-A/xrc/re.		PIN		UUT* FUNCTION
					INTERFACE SCHEMATICS						IJUT		
DT/J													
rp •	52	%	H/	i		2	HI3	l			1		<?f?l/of-C
TF •	51	26	M3	1		2	M4	1			2		C2101 (+)
TP '	So	Ik	K2,	1		J2	M2	+			o		R2101
		0/		1			N3	i			J		25 VDC IN
DC2A HI		ik	m	'I		2	P3	I					
Tr '	/ i		N5				N5	v	J		5		r 2101 - E
OCM fiX	*	%	W	1		A	P5	i.					
TF •	63	26	N7	i		2	M7	1.			6		16 VDC OUT
nr $3 Mf		JA	P7	i		X	P7	l	l				
WG HI			ai	J		X	G7	I					
TP •	22	if	C6	i		1	alp	±	S5^ 1				
TP '	riS'	0',	ni	1		X	DC	i	f		7		kzi.01
DC2 & HT-		26	G1	t		X	61	i.					
TP ·	Si	26	5M	l		z	5M	l	y		8		TpPOL$>£
									**k I.BK				
TP	VI		L1	l		2		i.			7		GROUND
PC2J U		ft	P4	1		Z	P4	i					
DC3A LO			P6	1		2	Pb	1					
fj.1 '* O i 7		n	G2			.1	(A	1					
W& /•(>			G8	i		Z	G8	1					
DC3B LO		26	P8	y		X	pi	i					

ATE FUNCTION	INTERFACE SCHEMATICS															UUT FUNCTION
	TP	J	PIN	P	CA1 & CA2	J	PIN	P	PIU ADAPTER	P	PIN	J		J	PIN	
AC-STD HI		32	A		CA2			2								
AC-STD LO		32	B					2								
	22	26	6C	1		2	6C	1			1			1	1	MON. AMP. IN
WG HI			7G				7G									
WG LO			8G		CA1		8G									
GND			8E				8E									
	33		1K				1K		33K		11				11	AUDIO AMP. IN
DC2A LO			4P				4P		R10 560 Ω							
DC2B LO			2G				2G									
DC3A LO			6P				6P				STUD				STUD	CKT. GND
	41		1L				1L		R9 150 Ω							
	48		8L				8L				8				8	MON. AMP. OUT
DC2A HI			3P				3P				2				2	+16 VDC
	59		3N				3N									
DC3A HI			5P				5P				9				9	+25.5 VDC
	61		5N				5N									
DC2B HI			1G				1G				13				13	+3.6 VDC
	25		1D				1D									
	43		3L				3L				3				3	CR5103-K
	44		4L				4L				4				4	R5117
	37		5K				5K				5				5	CR5103-A
	38		6K				6K				6				6	C5108
	47		7L				7L				7				7	+16 VDC
	34		2K				2K				10				10	CR5104-K

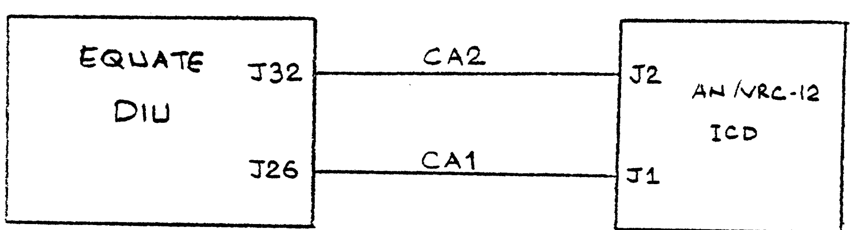


Figure 3.22 ICD Hookup Diagram

CHAPTER IV

Generation of a Test Program For Voltage Regulator Card-A210

The generation of a test program to diagnose and isolat single catastrophic failures in the A2100 voltage regulator card of the AN/VRC-12 radio is described in the following six sections. Section 1 presents the theory of operation for the circuit. This description closely follows the theor given in DMWR 11-5820-401 pages 34-35, and 3B.10-3B.12. Section 2 contains the input supplied to the top part of the NOPAL system. Each input option is briefly explained. An overview of the tables generated by the system is given in Section 3. The NOPAL specification of the tests based on these tables is explained in Section 4. The flowchart of th EQUATE ATLAS program which is generated from the NOPAL speci cation is described in Section 5. Finally in Section 6, the printouts obtained by running this program on EQUATE V or VI are exhibited and evaluated.

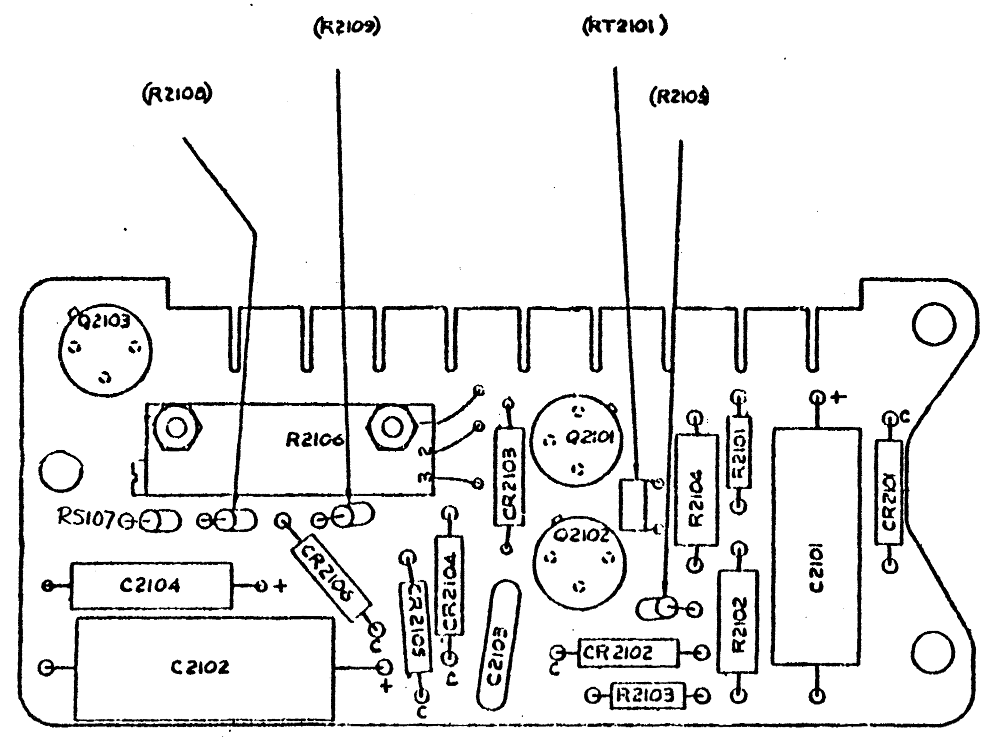


Figure 4.1 A2100 Voltage Regulator Circuit Card

4.1 Voltage Regulator Assembly-A2100: Theory of Operation

The voltage regulator card A2100 shown in Figure 4.1 provides a regulated output of 16 volts dc for circuits in the R-442/VRC (or the RT-246/VRC and RT-524/VRC) radiosets. The regulator maintains its 16-volt output over a wide range of current demands.

The A2100 circuit card contains circuitry to perform the following three functions: (A) 16-volt dc voltage regulation, (B) time delay circuit to operate a relay, and (C) an RC integrator and a small-signal rectifier. The operation of the circuitry for each function is explained below.

A. A simplied circuit schematic diagram of the voltage regulator portion of A2100 is shown in Figure 4.2.

The effective resistance of transistor Q202 (Q403) in series with the 25.5-volt dc supply drops the voltage to 16 volts dc for any current required by the external circuit. Diodes CR201 (CR40 CR202 (CR 406) and transistor Q202 (Q403) are not located on the voltage regulator assembly card-A2100. They are connected to the A2100 circuitry when the card is inserted into its slot in the radioset. If the current drawn from the regulator increases or decreases, the effective resistance of Q202 (Q403) is lowered or increased as necessary to maintain the output at 16 volts. This is done by controlling the transistor emitter-to-base bias voltag The emitter voltage is essentially fixed by the 25.5-volt dc supp The base voltage is controlled by the voltage drop across resisto R2104 and thermistor RT2101. The emitter current of Q2101 is controlled by its emitter-to-base bias voltage. Its collector is maintained out 16 volts dc since it is connected to the collector

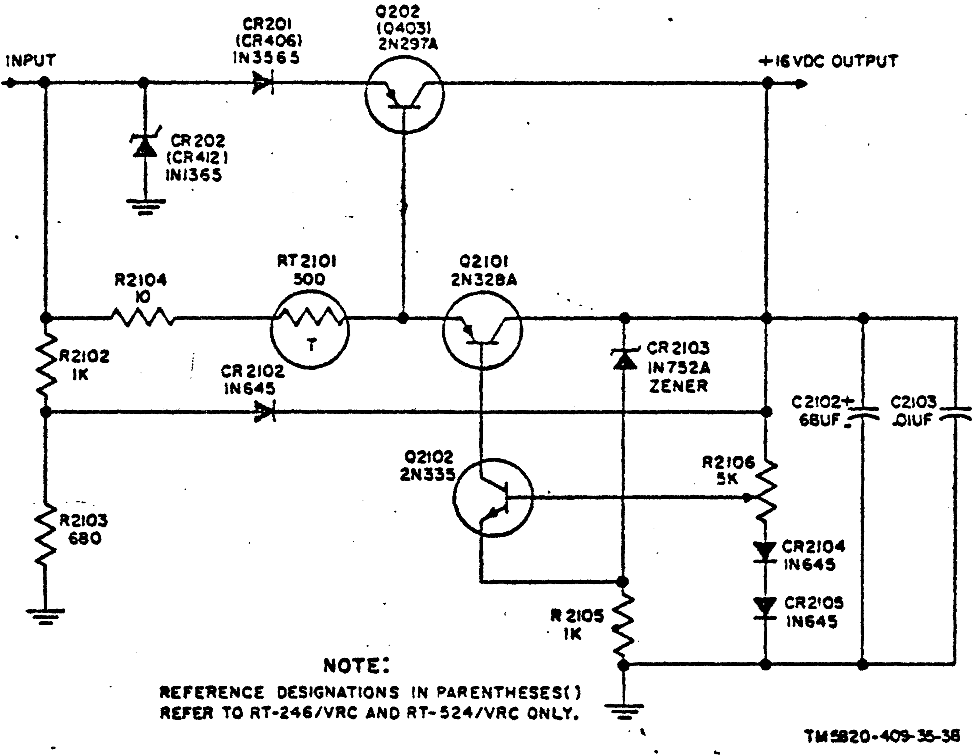


Figure 4.2 Voltage regulator, simplified schematic diagram.

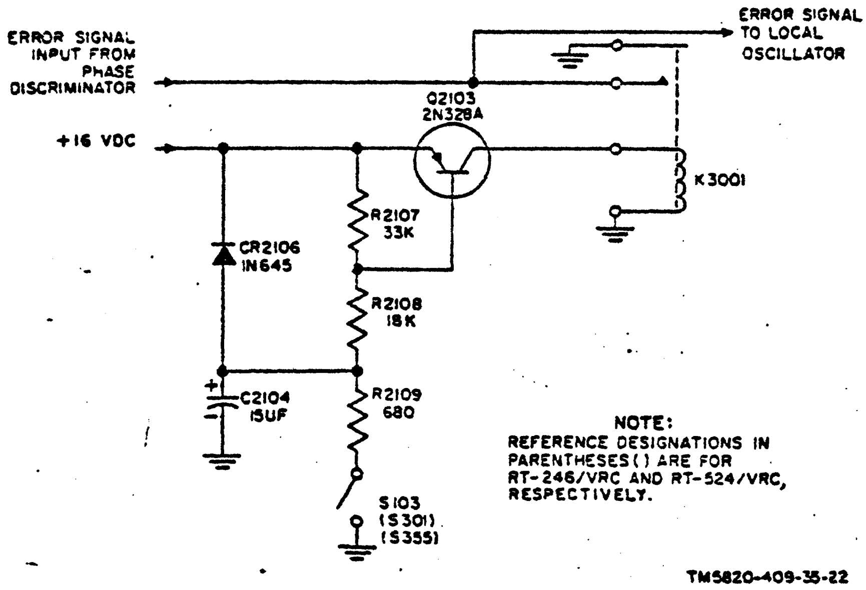


Figure 4.3 Time delay circuit, simplified schematic diagram.

generator on a motor vehicle. It starts shorting the spikes
above 39 volts. Capacitors C2102 and C2103 attenuate low and
high frequency ripple voltages, respectively.

B. Figure 4.3 shows the time delay circuit which is als
located on the A2100 circuit card assembly. This circuitry i
used to energize a relay which turns on and off the error sig
coming from the phase discriminator and going to the local os
This is done to prevent the local oscillator to lock on spuri
frequencies when the radio is being turned on and off and als
when megacycle tuning switch is being rotated. Relay K3001 a
switch S103 (S301, S355) are not physically located on the A2
card.

As power is applied, current flows through transistor Q2
and the coil of relay K3001. Relay K3001 energizes, error si
from the phase discriminator is provided, and capacitor C2104
begins to charge. When capacitor C2104 is charged, transisto
is biased to cutoff, relay K3001 deenergizes, and the ground
removed from the error signal and routed to the local oscilla
Resistor R2107 establishes the initial bias for transistor Q2
and, in combination with resistor R2108, determines the time
to charge capacitor C2104. Diode CR2106 enables quick discha
of capacitor C2104 when power is removed, thus assuming the c
of the time delay circuit in the event power to the equipment
switched off and on very quickly.

The time delay circuit also functions whenever megacycle
switch S103 closes. As the switch closes momentarily, capaci
discharges through resistor R2109 and the switch to ground.

Q202 (Q403). CR2103 is a 5.5-volt Zener diode which maintains the voltage on the emitter of transistor Q2102 at 5.5 volts lowe than the output voltage. Potentiometer R2106 establishes the ba voltage of Q2102. The effective resistance of Q2102 sets the ba voltage on Q2101 and thus controls its emitter current.

When the current requirement of the external circuit increa the collector voltage on Q207 (Q403) decreases. This decreases the emitter voltage of Q2102, decreasing its effective resistanc and lowering the base voltage on Q2101. The emitter current of Q2101 increases and lowers the base voltage on Q202 (Q403); thus decreasing its effective resistance. The voltage drop across Q202 (Q403) is reduced, and the output is increased to 16 volts

Diode CR2102 applies the voltage at the junction of resisto R2102 and R2103 to the base of Q2102 through potentiometer R2106 This action starts the regulator when power is first applied. A the output voltage reaches 16 volts dc, CR2102 is reverse-biased and effectively removed from the circuit.

Potentiometer R2106 compensates for variations in zener dio CR2103 and is used to manually adjust the regulator output to 16 volts dc.

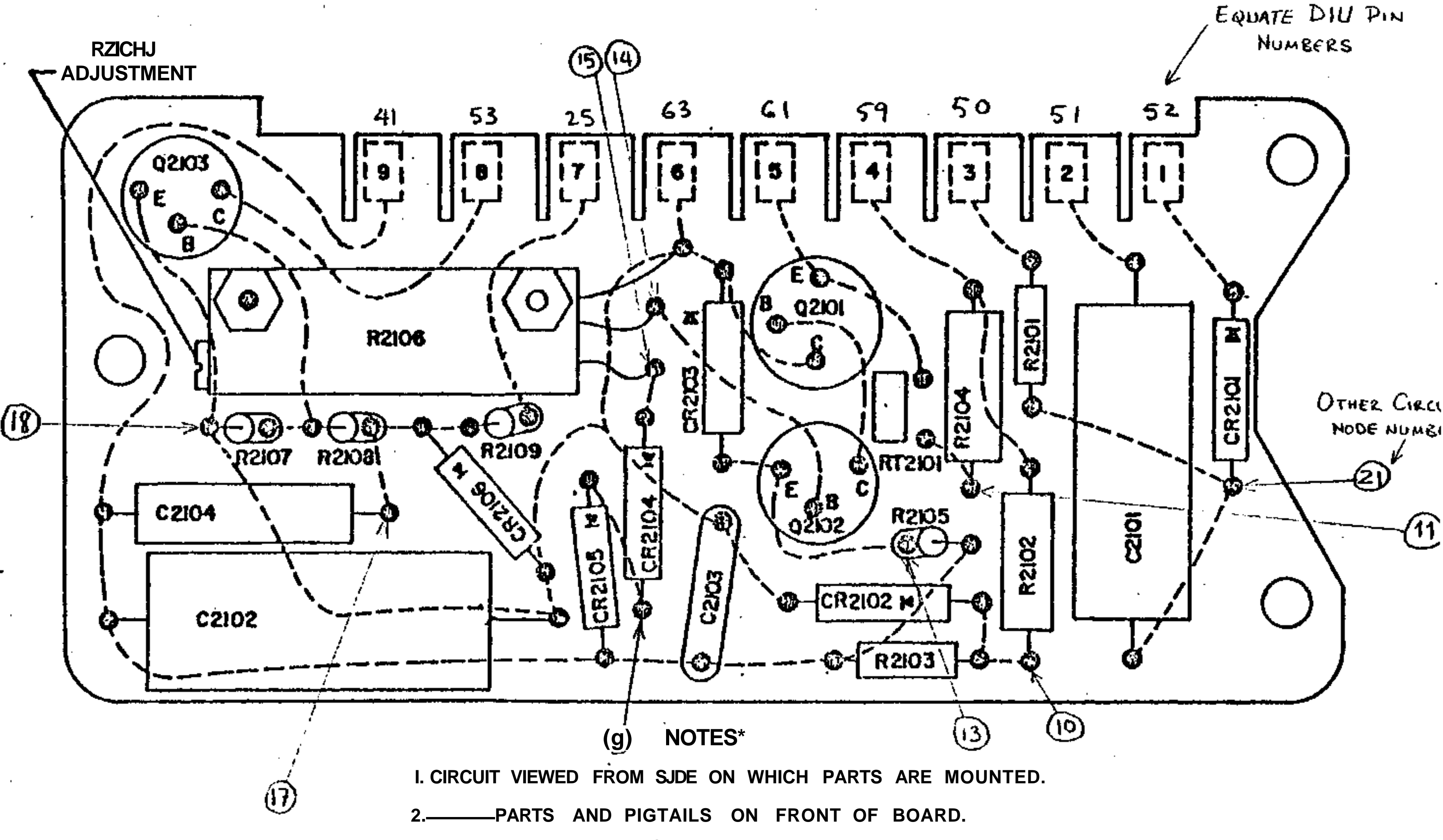
Diodes CR2104 and CR2105 compensate for variations in the emitter-to-base voltage of Q2102 caused by change of ambient and junction temperatures. Diode CR201 (CR406), resistor R2104, and thermistor RT2101 provide temperature compensation for transistor Q202 (Q403). Zener diode CR202 (Q412) protects the regulated 16 volt power supply lines from the intermittent spike which appear on the 25.5 volt supply line coming from a

capacitor C2104 is discharged, the sequence of events described above occurs. Switch S103 momentarily closes as the tuning gear train turns; this insures that the new crystal oscillators being selected provide the maximum output before the error signal is connected to the local oscillator.

C. The small subcircuit on the lower left hand side of Figure 4.4 is the RC subscircuit on the A2100 card which is not related to voltage regulation. Diode CR2101 performs rectificatic of an AC-signal. The output is routed through a large RC time constant circuit, resistor R2101 and capacitor C2101, back to the radioset. This circuit is referred to as the filter subscript in the remainder.

The complete circuit schematic of the circuitry contained on the A2100 card is shown in Figure 4.4. Figure 4.5 shows parts location and wiring diagram of the circuit card. The numbers enclosed in small circles point at the nodes of the circuit. Thes numbers are arbitrarily assigned to identify the nodes. The same node assignments are also used in Figure 4.4. The numbers in rectangles are actually printed on the circuit card for easy identification. The numbers above them are the EQUATE dedicated interface unit test points as they are routed to A2100 through the special VRC-12/EQUATE interface connecting device. These connections explained in more detail in the discussion of the interface in Section 3.4.

Figure 4.4 Circuit Schematic Diagram of A2100 Card



TM 8820-409-33-7«

Figure 4.5 Assembly A2100, Parts Location and Wiring Diagram.

4.2 NOPAL INPUT

The test program for the A2100 card is generated in two parts. The first program is for the filter subcircuit and the second program is for the voltage regulator and time delay circuit.

The complete input given to the top part of NOPAL to generate a test program for the filter subscript of the A2100 card is shown in Figure 4.6 and discussed in subsection A. The input which describes the voltage regulator and time delay circuit and its requirement is shown in Figure 4.7 and discuss in subsection B.

A. CIRCUIT DESCRIPTION AND REQUIREMENTS FOR THE FILTER SUBSC

The circuit description of the filter is shown in Figure 4.6. Resistor R2101 is 270 ohms and is incident on circuit nodes 0 and 21. In NAP2, node 0 is the ground refere node. Node 21 is arbitrarily named. Capacitor C2101 is 68μF and is incident on nodes 2 and 21. Diode QDR2101 (CR2101) is type 1N645 and is incident on nodes 21 and 3. The nodes 1,2 and 3 are also terminals on the edge connector of A2100. How node 21 is internal and not available unless probing of the c is allowed. (see Figures 4.3 and 4.4).

A diode model for IN645 has been previously stored in the model library number 2 of the NAP2 circuit analysis progr Hence its details need not be repeated in the circuit descrip A reference to the model by name enables the model to be retr from the library during simulation. The model for IN645 is included in the main circuit as a subscircuit by connecting i internal node 1 to node 21, and internal node 3 to node 1.

```
CIRCUIT_DESCRIPTION   A2100   DEFAULT  VOLTAGE REGULATOR
*CIRCUIT
: THIS CIRCUIT IS PART OF A2100 CIRCUIT BOARD
R2101  0   21   270  : FAILS
C2101 2   21   68UF : FAILS
QDR2101  21 = 1  1 = 3 : FAILS
*LIB2  D1N645
Q*
ROPEN1  1  0   10MEG
ROPEN2  2  0    10MEG
*MODIFY  1   0.1   0.1    R2101 C2101
*MODIFY   2   0.05  0.05   >
          QDR2101.RS  QDR2101.RB   QDR2101.CT   QDR2101.CD
*MODIFY   3    10.0  0.1   ROPEN1   ROPEN2
TEST_TERMINALS   J8   PC BOARD EDGE CONNECTOR
0   A21_3    GROUND
1   A21_1
2   A21_2
ACTEST_TERMINALS     J8     PC BOARD EDGE CONNECTOR
0   GND    GROUND
1   A21_1
2   A21_2
OBJECTIVES   STANDARD
 100.0%   DIAGNOSIS
  50.  2   AMBIGUOUS
  80.  4   AMBIGUOUS
ACCURACY MINIMAL
    0.50E-02                   ZERO DESCRIMINATION
    0.20E+02                   INACCURACY IN %
  3             SIGNIFICANT DIGITS
  1             SORT WITHIN TEST ONLY
  1             OPTIMIZE LOGIC
  1             MISSING FAILURES SAME AS NOMINAL
    1.00E+01   40.00E+04       RESISTANCE
    1.50E+01   01.00E+04       IMPEDANCE
    1.00E-03   01.00E+00       CURRENT
    0.50E+00   03.50E+01       VOLTAGE
   1   1
INITIAL_CONDITIONS   NOPOWER
END
```

Figure 4.6 NOPAL Input for A2100 Filter Subcircuit

The resistors ROPEN1 and ROPEN2 are not part of the circuit. They are included to prevent numerical analysis problems. Eventhough it is not always required to have at least two branches incident on each circuit node, it is a good practice not to leave any dangling branches for consistency. The valu of ROPEN1 and ROPEN2 are very high. For all practical purpos they can be considered open. The first "modify" statement specifies +-10% tolerance for R2101 and C2101. Diode QDR2101 has +-5 tolerance on most of its parameters: on short and bu resistances, and on transition and diffusion capacitances. ROPEN1 and ROPEN2 have +1000% and -10% tolerance. This wide tolerance is specified to show that these two resistors have no effect on circuit response.

All of the circuit nodes which are on the edge connector are declared to be test terminals. Node 21 is not made avail for probing. The objectives of fault isolation is held very high by requesting that all of the failures should be detecte (i.e. 100% diagnosis); furthermore one half of the failure mo should be isolated into groups containing no more than two possible failures (i.e. 50% of failures 2-ambiguously) and 80 of the failures should be isolated into groups containing no than four possibilities (i.e. 80% of failures, 4-ambiguously) In this particular subcircuit, this objective does not appear to be very meaningful. It is included here for uniformity wi other inputs. This is the standard objective which is used i all test programs.

Accuracy specifications state that (1) any measurement which is in the range -0.005 to 0.005 should be treated a z (2) any measurement taken can be as much as +-20% off from true value, (3) the test program should refer to stimuli an measurements using at most 3-significant difits, (4) minimu measureable resistance is 100 ohms, and maximum mesureable resistance is 400 Kohms, (5) minimum measureable impedance magnitude is 15 ohms, and maximum impedance is 10 kohms, (6 minimum current is 1 on A and maximum current is 1 A, (7) minimum voltage is 0.5 volt, maximum voltage is 35 volts.

After failure simulation, any failure which is not sim for a given test should be treated as resulting in nominal measurement. This option is actually not used in these pro It was specified here to prevent early termination of the t part in case of intentional omission of failure modes. The sort option is used for printing the tables according to av assertion or test sensitivity.

B. CIRCUIT DESCRIPTION AND REQUIREMENTS FOR THE VOLTAGE REGULATOR AND TIME DELAY SUBCIRCUITS

Figure 4.7 shows the circuit description of the voltag regulator and the time delay circuitry of the A2100 card. the circuit description first the semiconductor devices are connected. The terminals of the NPN and PNP transistors ar connected in the same sequence: collector, base and emitte The complete models of these devices are included in Append Potentiometer R210B is modelled as two separate fixed resis where R2106B is functionally dependent on R2106A. The valu

```
CIRCUIT_DESCRIPTION   A21C0   DEFAULT  VOLTAGE  REGULATOR
•CIRCUIT
FC / /    A   5.0E03   B   -1
QDR2102    10 = 1   6 * 3    :   FAILS
*LIB2     D1N645
a*
QQ21Q1     6 = 1   12 = 2    5 = 3     :   FAILS
*L132     TR2N329A
QQ2102    12 = 1  14 = 2   13 * 3      :   FAILS
*LI32      TR2N335
$*
&DR2103    13 = 3   6 = 1      :  FAILS
*LI82      21N752A
Q*
QDR2104    15 = 1  16 = 3      :    FAILS
*LI92     D1N645
Q*
QDR2105    1 6 * 1 0  =  3          :      FAILS
*LIB2     D1N645
Q*
R2104     4      11      13   :  FAILS
RT21G1     11     5      500      :      FAILS
R2102     4      10      1K :  FAILS
R2103     10     0      680 :  FAILS
R2105    13     0      1K   :   FAILS
RTAP     14     21      10      :  FAILS  OPEN
R2106A    21     15     3.44K    :  FAILS  SHORT
R21C6B    6      21      1*FC(R2106A)    :  FAILS  SHORT
C2102          {}   6<'UF  :  FAILS
C2103     6       C      •01UF    :     FAILS
QDR21C6   17 =: 1    6 = 3       :  FAILS
*L162      D1N645
a*
          17      0      15UF      :  FAILS
C2104     17      7      660      :  FAILS
R2109     17     15      18K      :  FAILS
R2108      i    18      33K      :  FAILS
R21Q7      8  =  115  = 2    6 = 3     :  FAILS
QQ2103    TR2N329A
*LIB2
RUUT1     8    0     1.83IC
RUUT2     6    C     33K
•MODIFY    1   C<35   0*05    R2104  R2102  R21C3  R2105  RT2101   >
           RTAP d2176A  R21068   C21Q2  C2103  C2104   >
           R2107  R2102  R21C9  RUUT1  RUUT2
•MODIFY      2     0*005    C.005  >
           032101.*?!  3Q21C1.R1  3Q210UIE  QQ2101.CET  QQ2101.CE0
          QQ2101.IN  CQ2131 •R2  QQ2101.IC  QQ2101.CCT  GQ2101.CCD  >
          UQ21C1.I1  QQ2101»RC   >
           Q22102.K?  QQ21G2.P.1  3C2102.IE  QCi2102.CET  GQ2102.CED
          QQ21G2.IN  J.221C2.R2  Q321C2.IC  UQ2^02.CCT  QQ2102.CCD   >
          aQ4IG2.II  UQ2102.RC   >
           QQ2103.RE)  QQ2103.R1  QQ2103.IE  QQ2103.CET  GQ2103.CED
```

Figure 4.7 NOPAL Input For A2100 Voltage Regul and Time Delay Subcircuits

```
        QQ2103.IN QQ2103.R2 QQ2103.IC QQ2103.CCT QQ2103.CCD  >
        QQ2103.II QQ2103.RC  >
       QDR2102.RS QDR2102.ID QDR2102.CT QDR2102.CD QDR2102.RB  >
       QDR2104.RS QDR2104.ID QDR2104.CT QDR2104.CD QDR2104.RB  >
       QDR2105.RS QDR2105.ID QDR2105.CT QDR2105.CD QDR2105.RB  >
       QDR2106.RS QDR2106.ID QDR2106.CT QDR2106.CD QDR2106.RB  >
     QDR2103.RS QDR2103.ID QDR2103.IZ QDR2103.CT QDR2103.CD  >
     QDR2103.RB
TEST_TERMINALS   J8   PC BOARD EDGE CONNECTOR
0   A21_9   GROUND
4   A21_4   MAIN POWER INPUT
5   A21_5   THERMISTOR CONNECTION
6   A21_6    REGULATED 16 VOLT OUTPUT
7   A21_7    S103 SWITCH POINT
8  A21_8     TIME DELAY OUTPUT
ACTEST_TERMINALS   J8   PC   BOARD EDGE  CONNECTOR
0   A21_9   GROUND
4   A21_4   MAIN POWER INPUT
5   A21_5   THERMISTOR CONNECTION
6   A21_6    REGULATED 16 VOLT OUTPUT
7   A21_7    S103 SWITCH POINT
8  A21_8     TIME DELAY OUTPUT
CONVERGENCE   CRITERION
 *MODIFY  V6=16,V5=20
OBJECTIVES   STANDARD
 100.0%   DIAGNOSIS
  50.  2   AMBIGUOUS
  80.  4   AMBIGUOUS
ACCURACY MINIMAL
    0.50E-02                      ZERO DESCRIMINATION
    0.10E+02                      INACCURACY IN %
  3               SIGNIFICANT DIGITS
  1              SORT WITHIN TEST ONLY
  1              OPTIMIZE LOGIC
  1              MISSING FAILURES SAME AS NOMINAL
    1.00E+01   40.00E+04          RESISTANCE
    1.50E+01   01.00E+04          IMPEDANCE
    1.00E-03   01.00E+00          CURRENT
    0.50E+00   03.50E+01          VOLTAGE
   1   0
ACBIAS    DC OPERATING POINT IS DECIDED BY THE FOLLWING DC SUPPLY
BEGIN  !A    ATTENTION OPERATOR:  UUT IS BEING POWERED NOW
RBIAS  4   0   0.1  E   25.5V
INITIAL_CONDITIONS   POWERUP
BEGIN  !A    ATTENTION OPERATOR:  UUT IS BEING POWERED NOW
RSUPPLY   4   0  0.1  E  25.5
END
END-INITIAL
```

Figure 4.7 NOPAL Input For A2100 Voltage Regulator and Time Delay Subcircuits (continued)

of R2106A is determined by an optimization simulation run requiring that R2106A should be adjusted such that the voltage at node 6 is equal to 16 volt dc. The simulation determines R2106A is 3.44 Kohm and R2106B is 1.56 Kohm (5 Kohm - 3.44 Kohl Both of the resistors may have +-5% tolerance. Resistors RUUT! and RUUT2 are not on the A2100 card. They are inside the AN/V3 interconnecting device. RUUT2 (33 Kohm) is not documented on the original ICD description. It was discovered during testin< and added to the interface schematic shown in Figure 3.20. Th: leakage resistor discharges capacitor C2102 after a stimulus is removed from the card. RUUT2 is a load resistor for the time delay circuit. It effectively puts a load to ground on tl collector of transistor Q2103. All resistors and capacitors a; assigned +-5% tolerance. All diode and transistor model param< are assigned -f--Q.5% tolerance. Their tolerance specifications were deduced from semiconductor data books. These tolerances may result in up to 20-30% tolerance on transistor gain (beta) characteristics.

The edge connections are assigned the same circuit node numbers. In addition to the edge connectors, circuit nodes 15 18 are used as probe test points. In the current implementati< of the top part of NOPAL, there are no explicit provisions to generate special instructions to the operator to make the required connection. The probe message and the required ATLAS command is implemented in the OHMMETER, ZMETER or VOLTMETER functions. This is done by assigning the probe points to be connections points which are beyond the EQUATE'S capability, tl

during execution, these cases are intercepted in the function prologue code to branch to the appropriate instructions to issue the probe message and to use the "PROBE" connection. The convergence crition (16 volts dc on node 6 and 25 volts dc on node 20) is not required. It is specified only to speed up th simulation and prevent possible numerical (no-convergence) pro Experience with failure simulation indicates that solutions ar considerably faster when the initial conditions for non-linear circuits are started from the nominal voltage levels rather th from all node voltages and branch currents at zero. All circu analysis programs start the numerical solutions from zero leve unless different initial conditions are specified by the user.

The remainder of the requirements listed in Figure 4,7 ar identical to those described in the previous subsection.

4.3 Evaluation of Tables Generated

The tables generated to the top part of NOPAL are evaluat in this section. The dicussion of the two subcircuits are don separately. The tables generated for the filter subcircuit a: discussed fully in Subsection A. In Subsection B, the tables generated for the remaining circuits are discussed however the complete table listings except the shortest significant ones a not included due to their length. The complete tables are available as computer listings and on a computer tape accompan this report.

A. NOPAL Tables For The Filter Subcircuit

The first table generated from the user provided input is failure dictionary. Table 4.1 shows the failure dictionary fo the filter subcircuit. There are 7 failure modes which the ci may have. Failure identification number 1 is not actually a failure, it is the nominal state of the circuit. It is includ in table for completeness. Each component has two failure mod as described in Section 3.2. This failure dictionary is simpl a document of the failure modes which are analyzed by the top In digital testing literature, the term 'failure dictionary[1] a includes the data which is called the 'failure symptoms[1] in th NOPAL system. This information is not apart of NOPAL failure dictionary.

Even though it is theoretically possible, it is very unli to have resistors failing by the shorting of their terminals. Initially in the course of this study, it was decided to inves the symptoms of failure due short of resistors to determine whether or not they could be isolated. It was observed that i many cases short of resistors could not be identified, i.e., t

FAILURE DICTIONARY --- (PAGE 1)

ID.	COMPONENT NAME	FAILURE FUNCTION	NODES	CHANGE	TYPE	PARAMETER	REMARK (VALUE)	REMARK (ALIAS)	REMARK (INDEX)
1	ALL_COMPS	NONE		NONE	NONE	NOMINAL	NOMINAL	NOMINAL	0
2	R2101	OPEN	0 21	VALUE	RESISTOR	1.0E9	270	OPEN	0
3	R2101	SHORT	0 21	VALUE	RESISTOR	1.0E0	270	SHORT	0
4	C2101	OPEN	2 21	TOPOLOGICAL	RESISTOR	1.0E9	68UF	OPEN	0
5	C2101	SHORT	2 21	TOPOLOGICAL	RESISTOR	1.0E0	68UF	SHORT	0
6	QDR2101	OPEN	21 1	TOPOLOGICAL	DEFINED	1.0E9	D1N645	OPEN	0
7	QDR2101	SHORT	21 1	TOPOLOGICAL	DEFINED	1.0E0	D1N645	SHORT	0

Table 4.1 A2100 - Filter Subscircuit Failure Dictionary

circuit behaves as if it were normal. There were several exceptions to this behavior, i.e. resistors which are involved in biasing and feedback circuits usually serve as voltage dividers, hence they effect circuit behavior significantly. All of these failures can be picked up. However, many resistors are included as safety devices for limiting the current when large amount of current is drawn. Hence under normal conditions their failure by shorting does not affect the operation of the circuit Due to these reasons, in addition to the statistics published by industry indicating very seldom occurance of such failures, the final test programs which are generated for these circuits exclu resistor shorted failures. Resistor short failures are included in the analysis until the generation of failure symptom tables.

In reports presented here, and on the accompanying computer tape, they are dropped from further investigation. If it become desirable to include any or all of these failures, new ambiguity analysis, optimization, NOPAL specification and ATLAS program generation steps can be easily performed including the additiona failures. The operations described above amount to only one job on the computer.

Table 4.2 is the test limit and diagnosis table which conta the assertions created from the failure symptom table. This tab contains 8 different tests with an average of 2 assertions per t A total of 17 assertions are created. The actual identification and the test points involved in these tests are available in oth reports not shown here. These assertions are created slightly differently from the original version of the top part of NOPAL.

1	1	1	R	METER	1	3.19000E 05	1.20000E 58	1.74134E-06	1 1 1 1 1 1 0
2	1	1	R	METER	2	1.94000E 02	3.70000E 02	1.57797E-04	0 0 0 0 0 0 1
3	2	1	R	METER	1	3.19000E 05	1.20000E 58	1.74148E-06	1 1 1 1 0 1 1
4	2	1	R	METER	2	1.94000E 02	3.70000E 02	1.57795E-04	0 0 0 0 1 0 0
5	3	1	R	METER	1	3.19000E 05	1.20000E 58	1.29205E-06	1 1 1 1 0 1 1
6	3	1	R	METER	2	2.03000E 02	3.22000E 02	1.13803E-04	0 0 0 0 1 0 0
7	4	1	R	METER	1	3.19000E 05	1.20000E 58	1.55367E-07	1 1 1 1 1 1 0
8	4	1	R	METER	2	1.94000E 02	3.70000E 02	1.40891E-05	0 0 0 0 0 0 1
9	5	1	R	METER	1	3.19000E 05	1.20000E 58	1.55489E-07	1 1 1 1 0 1 1
10	5	1	R	METER	2	1.94000E 02	3.70000E 02	1.40890E-05	0 0 0 0 1 0 0
11	6	1	R	METER	1	3.19000E 05	1.20000E 58	7.85078E-08	1 1 1 1 1 1 1
12	7	1	R	METER	1	4.48000E 02	7.54000E 02	8.47967E-05	1 0 0 1 1 0 0
13	7	1	R	METER	2	1.94000E 02	3.70000E 02	1.35800E-04	0 0 1 0 0 0 1
14	7	1	R	METER	3	3.19000E 05	1.20000E 58	1.73209E-06	0 1 0 0 0 1 0
15	8	1	Z	METER	1	1.72000E 02	3.90000E 02	0.00000E 00	1 0 0 0 1 1 1
16	8	1	Z	METER	2	6.42000E-01	1.80000E 01	0.00000E 00	0 0 1 0 0 0 0
17	8	1	Z	METER	3	8.00000E 03	1.20000E 56	0.00000E 00	0 1 0 1 0 0 0

A test may have at most three assertions: (1) a nominal assert, giving the expected nominal range of measurement and identifyin all components which result in this measurement, (2) a low asse giving the range of measurement and indentifying the failure mo for which the measurement is less than the nominal, and (3) a high assertion giving the range of measurement and identifying failure modes which result in a measurement higher than the nominal. In certain cases either the low or the high assertion may not be present. This is due to the fact that all measuremei have a low and a high measureable limit. It is physically not possible to get a reliable measurement beyond these limits. In these assertions, if a measurement is above 400 Kohms, it is replaced by a very large number. Then during code generation a corresponding,assertion is created requiring that the measure be greater than the lower limit with no restriction on the high limit. Similarly the converse is done for the low-assertions.

The following additional observations are noted: (1) When a test has a single assertion, it contains no useful fault isol information. (2) When there are two assertions; the first one is the nominal, and the second one may be either the low or the high assertion. (3) Where there are three assertions, the first one is the nominal, the second one is the low, and third is the high assertion.

Table 4.3 is a condensed form of Table 4.2. It is obvious that test 6.1 (stimulus 6, measurement 1) provides no fault

SE(i	STIM		TARGET VARIABLE	DESI6	LOWER LIMIT	UPPER LIMIT	SENSITIVITY	MULTIPLE VALUED DIAGNOSIS MATRIX
1	1	1	R METER	2	3.19000E 05	1.20000E 58	2.40351E-05	1 i 1 1 1 1 2
3	2	1	R METER	2	3.19OOOE 05	1.20000E 58	2.40348E-05	1 1 1 1 2 1 1
5	3	1	H METER	2	3.19000E 05	1.20000E 58	1.7365DE-O5	1 i 1 1 2 1 1
7	4	1	R METER	2	3.19000E 05	1.20000E 58	2.14590E-06	i 1 1 1 1 1 2
9	5	1	R METER	2	3.19OOOE 05	1.20000E 58	2.U599E-06	i i 1 1 2 t 1
11	6	1	R METER	1	3.19003E 05	1.20030E 58	7.85O78E-O8	i i 1 1 1 1 1
12	7	1	R METER	3	4.4feO00E 02	7.54000E 02	7.56363E-05	1 3 2 1 1 3 2
15	8	1	*i* METER	3	1.72000E 02	3.90000E 02	O.OOOOOE 00	1 3 2 3 1 1 1

Table 4.3 Multiple Valued Diagnosis Matrix and Test Circuits Table

isolation information; tests (2.1, 3.1, 5.1) and (1.1, 4.1) provide the same fault isolation information.

The ambiguity report shown as Table 4.4 indicates that all failures and the nominal mode can be uniquely identified. Fail short of R2101 has been dropped in this phase.

The first step of optimization gets rid of the redundant test setups. It retains only the minimum number of tests which are essential to achieve the same level of fault isolation whic was indicated during the ambiguity analysis phase. This optimi is based entropy (information content) only (see Table 4.5). T the tests selected have an interesting property. The first tes selected (7.1) has a very general fault isolating capability. It divides all possible failures into three classes where each class has nearly equal number of failures. The next test (8.1) divides these classes into smaller classes. This type of fault isolation design is commonly referred to as the top-down methodology. During this optimization phase, it is determined that only 3 out of the 8 original tests are sufficient to provi the same fault isolation capability.

The next table (Table 4.6) shows how the assertions of the remaining three tests can be put together with conjunctions to select diagnoses. Diagnosis 6 (short of CR 2101) and Diagnosis (short of C2101) are selected upon the completion of a single assertion. Diagnosis 2 (Open of R2101), Diagnosis 3 (Open of C2101), Diagnosis 5 (Open CR2101) can be selected only after th two required tests are performed. Diagnosis 1 (all component nominal) is selected after all three tests are performed.

AMBIGUITY REPORT (PAGE 1)

EQUIVALENCE CLASS	K-AMBIGUITY	FAULT ISOLATION PERCENTAGE		FAILURE MODES INCLUDED
		CLASS	CUMULATIVE	
NOMINAL	1	16.7%	16.7%	ALL COMPONENTS NOMINAL
2	1	16.7%	33.3%	OPEN(R2101).
3	1	16.7%	50.0%	OPEN(C2101).
4	1	16.7%	66.7%	SHORT(C2101).
5	1	16.7%	83.3%	OPEN(QDR2101).
6	1	16.7%	100.0%	SHORT(QDR2101).

Table 4.4 Ambiguity Report

FAULT ISOLATION SUMMARY

DESIRED AND ACHIEVED LEVEL OF CUMULATIVE
FAULT ISOLATION PERCENTAGE

K-A*3IGUITY	DESIRED C.F.L«P	ACHIEVED G.F.X.F.	CLASS f•I.P.	NUMBER
1	0.C2	103.0%	100.02	6
2	50.02	100.02	0.02	0 *
4	50.02	103.02	0.02	0 - t

MUM3EP 3F FAILURE MODES : 7
NUM3ER OF EQUIV. CLASSES : t
DESIRED LEVEL OF DIAGNOSIS: 100.OX
ACHIEVED LEVEL OF DIAGNOSIS: 100.02
FAULT ISOLATION IS SATISFACTORY.

Table 4.4 Ambiguity Report (continued)

```
FAILURE MODES                               1  2  3  4  5  6  7

SEQ  ( 12) STIMULUS (  7) MEASUREMENT (  1) ASSERTION (  3)
NUMBER OF TESTS USED              :   1
NUMBER OF EQUIVALENCE CLASSES     :   3
ENTROPY REQUIRED FOR ISOLATION    :   2.807
CURRENT ENTROPY                   :   1.557
CAPACITY (THEORETICAL MAX.)       :   1.585
EQUIVOCATION                      :   1.251
EFFECTIVENESS                     :   0.982
MEMBERSHIP IN EQUIV. CLASSES        1  2  3  1  1  2  3

SEQ  ( 15) STIMULUS (  8) MEASUREMENT (  1) ASSERTION (  3)
NUMBER OF TESTS USED              :   2
NUMBER OF EQUIVALENCE CLASSES     :   6
ENTROPY REQUIRED FOR ISOLATION    :   2.807
CURRENT ENTROPY                   :   2.522
CAPACITY (THEORETICAL MAX.)       :   2.585
EQUIVOCATION                      :   0.286
EFFECTIVENESS                     :   0.976
MEMBERSHIP IN EQUIV. CLASSES        1  2  3  4  1  5  6

SEQ  (  3) STIMULUS (  2) MEASUREMENT (  1) ASSERTION (  2)
NUMBER OF TESTS USED              :   3
NUMBER OF EQUIVALENCE CLASSES     :   7
ENTROPY REQUIRED FOR ISOLATION    :   2.807
CURRENT ENTROPY                   :   2.807
CAPACITY (THEORETICAL MAX.)       :   2.807
EQUIVOCATION                      :   0.000
EFFECTIVENESS                     :   1.000
MEMBERSHIP IN EQUIV. CLASSES        1  2  3  4  5  6  7
```

INDIVIDUAL AND JOINT ENTROPY VALUES

SEQ	STIM	MEAS	ASSE	ENTROPY	JOINT ENTROPY	EQUIV. CLA
7	7	1	12	1.557	1.557	3
8	8	1	15	1.379	2.522	6
2	2	1	3	0.592	2.807	7
1	1	1	1	0.592	2.522	6
3	3	1	5	0.592	2.807	7
4	4	1	7	0.592	2.522	6
5	5	1	9	0.592	2.807	7
6	6	1	11	0.000	2.522	6

OUT OF   8 CANDIDATE TESTS   3 ARE RETAINED

Table 4.5 A2100 - Test Setup Optimization Report

```
INPUT IS A MULTIPLE VALUED DIAGNOSIS MATRIX
   - NO NEGATIONS OF ASSERTIONS WILL BE GENERATED

NUMBER OF TESTS (OR ASSERTIONS) PER DIAGNOSIS WILL BE MINIMIZED


DIAGNOSIS  :   1
TEST( 12)  STIMULUS(  7)  MEASUREMENT(  1)  ASSERTION(  1)  LOGIC(
TEST( 15)  STIMULUS(  8)  MEASUREMENT(  1)  ASSERTION(  1)  LOGIC(
TEST(  3)  STIMULUS(  2)  MEASUREMENT(  1)  ASSERTION(  1)  LOGIC(

DIAGNOSIS  :   2
TEST( 14)  STIMULUS(  7)  MEASUREMENT(  1)  ASSERTION(  3)  LOGIC(
TEST( 17)  STIMULUS(  8)  MEASUREMENT(  1)  ASSERTION(  3)  LOGIC(

DIAGNOSIS  :   3
TEST( 12)  STIMULUS(  7)  MEASUREMENT(  1)  ASSERTION(  1)  LOGIC(
TEST( 17)  STIMULUS(  8)  MEASUREMENT(  1)  ASSERTION(  3)  LOGIC(

DIAGNOSIS  :   4
TEST(  4)  STIMULUS(  2)  MEASUREMENT(  1)  ASSERTION(  2)  LOGIC(

DIAGNOSIS  :   5
TEST( 14)  STIMULUS(  7)  MEASUREMENT(  1)  ASSERTION(  3)  LOGIC(
TEST( 15)  STIMULUS(  8)  MEASUREMENT(  1)  ASSERTION(  1)  LOGIC(

DIAGNOSIS  :   6
TEST( 13)  STIMULUS(  7)  MEASUREMENT(  1)  ASSERTION(  2)  LOGIC(

TOTAL NUMBER OF TEST SETUPS        :   3
TOTAL NUMBER OF ASSERTIONS         :   8
SHORTEST TEST SETUP                :   1
LONGEST  TEST SETUP                :   3
SHORTEST CONJUNCTION               :   1
LONGEST  CONJUNCTION               :   3
```

Table 4.6 A2100 - Logic Optimization Report

B. NOPAL Tables For The Voltage Regulator and Time-Delay Circu

The failure dictionary for the circuit contains 54 failure modes. All applicable default (single catastrophic) failures a described in Section 3.2 are included. 9 failures are due to resistor shorts. It is assumed that the components and cabling of the interconnecting device cannot have any failures. The complete failure dictionary is contained in the accompanying computer tape and listings. It is not included in this report due to its length.

The binary and multiple valued diagnosis matrix and assertions tables are also not included in this report. In the reports there are 34 test setups and 84 assertions. On the ave there are 2.5 assertions per test.

The ambiguity report (Table 4.7) shows how 45 failure mode are isolated in 27 equivalence classes. The failures in each equivalence class have identical electronic behavior. In the no-diagnosis class (i.e. nominal) the open failure of zener dic CR2103 could not be diagnosed. This is due to the fact that given the light loading of the circuit, the potentiometer can adjust the output to 16 volts. However the short failure of th zener can be isolated uniquely. The open failure of the capaci C2103 (0.01μF) could not be diagnosed because it is in parallel with a relatively large capacitor C2102 (68μF) which has +-5% tolerance. It is not possible to distinguish between the open (class 10) and short (class 11) failures of diodes CR2104 and CR2105. These diodes are one of the same type and are connecte

AMBIGUITY REPORT (PAGE 1)

EQUIVALENCE CLASS	K-AMBIGUITY	FAULT ISOLATION PERCENTAGE		FAILURE MODES INCLUDED
		CLASS	CUMULATIVE	
NOMINAL	1	2.3%		ALL COMPONENTS NOMINAL
NO-DIAGNOSIS	3	6.8%		NOMINAL(ALL_COMPS), OPEN(QDR2103), OPEN(C2103).
2	1	2.3%	2.3%	OPEN(QDR2102).
3	2	4.5%	6.8%	SHORT(QDR2102), EC_SHORT(QQ2101).
4	7	15.9%	22.7%	COLL_OPEN(QQ2101), BASE_OPEN(QQ2101), COLL_OPEN(QQ2102), BASE_OPEN(QQ2102), EMIT_OPEN(QQ2102), OPEN(R2105), OPEN(RTAP).
5	2	4.5%	27.3%	EMIT_OPEN(QQ2101), BE_SHORT(QQ2101).
6	2	4.5%	31.8%	BC_SHORT(QQ2101), EC_SHORT(QQ2102).
7	1	2.3%	34.1%	BC_SHORT(QQ2102).
8	1	2.3%	36.4%	BE_SHORT(QQ2102).
9	1	2.3%	38.6%	SHORT(QDR2103).
10	2	4.5%	43.2%	OPEN(QDR2104), OPEN(QDR2105).
11	2	4.5%	47.7%	SHORT(QDR2104), SHORT(QDR2105).

[illegible]

EQUIVALENCE CLASS	K-AMBIGUITY	[illegible] PERCENTAGE: CLASS	[illegible] PERCENTAGE: CUMULATIVE	[illegible]
12	2	4.[illegible]	[illegible].3%	[illegible]EN(R2104), O[illegible]EN[illegible].
13	1	2.[illegible]	[illegible].5%	O[illegible]N(R2102).
14	1	2.3%	[illegible]	OPEN(R2103).
15	1	2.3%	59.1%	OPEN(C[illegible]102).
16	2	4.5%	63.6%	SHORT(C[illegible]102), SHORT(C[illegible]03).
17	1	2.3%	65.9%	OPE[illegible]106).
18	1	2.3%	[illegible]	SHORT(Q[illegible]106).
19	1	2.3%	[illegible].5%	[illegible](C[illegible]104).
20	1	2.3%	72.7%	SHORT(C2104).
21	1	2.3%	7[illegible]0%	[illegible](R2100).

EQUIVALENCE CLASS	K-AMBIGUITY	FAULT ISOLATION PERCENTAGE		FAILURE MODES INCLUDED
		CLASS	CUMULATIVE	
22	2	4.5%	79.5%	OPEN(R2108), OPEN(R2107).
23	1	2.3%	81.8%	COLL_OPEN(QQ2103).
24	2	4.5%	86.4%	BASE_OPEN(QQ2103), EMIT_OPEN(QQ2103).
25	1	2.3%	88.6%	BC_SHORT(QQ2103).
26	1	2.3%	90.9%	BE_SHORT(QQ2103).
27	1	2.3%	93.2%	EC_SHORT(QQ2103).

Table 4.7 A2100-Voltage Regulator and Time Delay Circuit Ambiguity Report (continued)

FAULT ISOLATION SUMMARY

DESIRED AND ACHIEVED LEVEL OF CUMULATIVE
FAULT ISOLATION PERCENTAGE

K-AMBIGUITY	DESIRED C.F.I.P.	ACHIEVED C.F.I.P.	CLASS F.I.P.	NUMBER
1	0.0%	36.4%	36.4%	16
2	50.0%	77.3%	40.9%	9
3	50.0%	93.2%	0.0%	0
7	80.0%	93.2%	15.9%	1

NUMBER OF FAILURE MODES : 45
NUMBER OF EQUIV. CLASSES : 27
DESIRED LEVEL OF DIAGNOSIS: 100.0%
ACHIEVED LEVEL OF DIAGNOSIS: 93.2%
FAULT ISOLATION IS NOT SATISFACTORY.

Table 4.7 A2100-Voltage Regulator and Time Delay Circuit Ambiguity Report (continued)

in series. The failures could be isolated to a single diode if probing of their common connection point was allowed. Th open failure of resistor R2104 and thermistor RT2101 could n be distinguished from each other for the same reason.

The complete optimization report of the test setup is n included due to its length. Only the summary of the process is shown in Table 4.8. The tests selected in this optimizat phase exhibit a top-down fault isolation capability as discu in previous subsection. The process is initiated with 34 ca tests. Only 13 of these tests are sufficient to achieve the same level of fault isolation.

The final report (Table 4.9) shows how 37 assertions of 13 remaining tests can be used in conjunctions to select the diagnoses.

The selection of most of the diagnoses is very quick (i they depend only one or two assertions. But the selection o diagnoses such as diagnosis 5,9 and 27 are not obvious at al They can be selected only after performing 4 or 5 tests. If complicated selection logic had to be done manually, it woul been very difficult to make the choices. These cases highli the benefits of automating the process.

INDIVIDUAL AND JOINT ENTROPY VALUES

SĕG	STIM	MEAS	A$$E	ENTROPY	JOINT ENTROPY	EQUIV. CLASS
23	21	3	58	1 .084	1 .084	3
10	10	1	23	1.011	2.035	7
13	13	1	31	0.803	2.703	11
33	25	1	79	0.614	3.199	15
16	16	1	39	0.725	3.599	19
34	26	1	82	0.605	3.912	22
18	.18	1	45	0.825	4.206	25
17	17	1	42	0.455	4.465	29
6	6	1	12	0.361	4.546	30
19	19	1	48	0.133	4.622	31
20	20	1	50	0.361	4.694	32
1	1	1	1	0*455	4.755	33
21	21	1	53	0.310	4.806	34
2	2	1	4	0.361	4.806	34
3	3	1	£	0.650	4.806	34
4	4	1	i	0.614	4.806	34
5	5	1	11	0.000	4.306	34
7	7	1	15	0.8c9	4.806	34
3	8	1	15	0.747	4.806	34
9	9	1	21	0.229	4.80S	34
11	11	1	ci	0.854	4.806	34
12	12	1	29	0.361	4.806	34
14	14	1	34	0.650	4.806	34
15	15	1	36	0.614	4.806	34
22	21	2	55	1.071	4.306	34
24	21	4	d	0.310	4.806	34
25	21	5	63	0.361	4 .806	34
26	22	1	66	0.31Q	4.806	34
17	22	2	6B	0.133	4.806	34
28	22	3	70	0.000	4.306	34
29	22	4	71	0.133	4.306	34
30	22	5	73	0.133	4.806	34
31	23	1	75	0.229	4.806 *	34
32	24	1	77	0.229	4.806	34

OUT OF 34 CANDIDATE TESTS 13 ARE RETAILED

Table 4.8 A2100 Test Setup and Optimization Summary Report

```
C      INPUT IS A MULTIPLE VA LUEo DIAGNOSIS MATRIX
          - NO NEGATIONS <OF ASSERTIONS taILL BE GENERATED

C.
       NUMBER OF TESTS COR ASSERTIONS) PER DIAGNOSIS WILL BE MINIMIZED

C

       DIAGNOSIS    :   1
(      TESTC  55>   STIMULUSC  21)  MEASUREMENTC  3)  ASSERTIONC  1)  LOGI CU )
       TESTC  23)   STIMULUSC  10)  MEASUREMENTC  D   ASSERTIONC  1)  LOGICCS )
       TESTC  31)   STIMULUSC  13)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
(      TESTC  79)   STIMULUSC  25)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
       TESTC  39)   STIMULUSC  16)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
       TESTC  52)   STIMULUSC  26)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
(      TESTC  42)   STIMULUSC  17)  MEASUR£M£NTC  1)  ASSERTIONC  1)  LOGICCS )
       TSSTC  43)   STIMULUSC  19)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
       TESTC  50)   STIMULUSC  20)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
(
       DIAGNOSIS    :   2
       TESTC  23)   STIMULUSC  10)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
I      TESTC  41)   STIMULUSC  16)  MEASUREMENTC  1)  ASSERTIONC  3)  LOGICCS )

       DIAGNOSIS    :   3
       TESTC  24)   STIMULUSC  10)  MEASUREMENTC  1)  ASSERTIONC  2)  LOGICCS )
       TESTC  40)   STIMULUSC  16)  MEASUREMENTC  1)  ASSERTIONC  2)  LOGIcU )

(      DIAGNOSIS    2   4
       TESTC  59)   STIMULUSC  21)  MEASUREMENTC  3)  ASSERTIONC  2)  LOGICCS )
       TESTC  47)   STIMULUSC  18)  MEASUREMENTC  1)  ASSERTIONC  3)  LOGICCS )
(
       DIAGNOSIS    :   5
       TESTC  59)   STIMULUSC  21)  MEASUREMENTC  3)  ASSERTIONC  2)  LOGICCS )
       TESTC  23)   STIMULUSC  10)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
       TESTC  39)   STIMULUSC  16)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
       TESTC  45)   STIMULUSC  16)  MEASUREMfcNTC  1)  ASSERTIONC  1)  LOGICCS )
(
       DIAGNOSIS    :   6
      'TESTC  23)   STIMULUSC  10)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
       TESTC  40)   STIMULUSC  16)  MEASUREMENTC  1)  ASSERTIONC  2)  LOGICCS )
       TESTC  45)   STIMULUSC  18)  MEASUREMENT   1)  ASSERTIONC  1)  LOGICCS. )

       DIAGNOSIS    :   7
       TESTC  53)   STIMULUSC  21 ) MEASUREMENTC  3)  AssERTjOfoC 1.) LOGICCS )
       TESTC  47)   STIMULUSC  1£)  MEASUREMENTC  1)  ASSERTIONC  3)  LOGICCS )
(
       DIAGNOSIS    :   8
       TESTC  59)   STIMULUSC  21)  MEASUREMENTC  3)  ASSERTIONC  2)  LOGICCS )
(      TESTC  51)   STIMULUSC  25)  MEASUREMENTC  1)  ASSERTIONC  3)  LOGICCS )

       DIAGNOSIS    :   9
       TESTC  59)   STIMULUS( 21)   MEASURfMCNTC  3)  ASSERTIONC  2)  LOGICCS )
       TESTC  24)   STIMULUSC  10)  MEASUREMENTC  1)  ASSERTIOMC  2)  LOGICCS )
       TESTC  31)   STIMULUSC  13)  MEASUREKSNTC  1)  ASSERTIONC  1)  LOGICCS )
(      TESTC  79)   STIMULUSC  25)  MEASUREMENTC  1)  ASSERTIONC  1)  LOGICCS )
       TESTC  45)   STIMULUSC  U )  MEASUR£MENTC  1)  ASSERTIONC  1)  LOGICCS )

(      DIAGNOSIS    :  10
       TESTC  53)   STIMULUS( 21 )  MEASUREMENTC  3)  ASSERTION   1)  LOGICCS )
       TESTC  31)   STIMULUSC  25)  MEASUREMENTC  1)  ASSERTIONC  3)  LOGICCS )
(
       DIAGNOSIS    :  11
       TESTC  50)   STIMULUSC  25)  MEASUREMENTC  1)  ASSERTIONC  2)  LOGICCS )
(
       DIAGNOSIS    :  12
```

Table 4.9 A2100 Logic Optimization Report

```
TEST( 14)   STIMULUS(  6)   MEASUREMENT(  1)   ASSERTION(  3)   LOGIC(& )

DIAGNOSIS   :  13
TEST( 59)   STIMULUS( 21)   MEASUREMENT(  3)   ASSERTION(  2)   LOGIC(& )
TEST(  3)   STIMULUS(  1)   MEASUREMENT(  1)   ASSERTION(  3)   LOGIC(& )

DIAGNOSIS   :  14
TEST( 58)   STIMULUS( 21)   MEASUREMENT(  3)   ASSERTION(  1)   LOGIC(& )
TEST( 25)   STIMULUS( 10)   MEASUREMENT(  1)   ASSERTION(  3)   LOGIC(& )

DIAGNOSIS   :  15
TEST( 49)   STIMULUS( 19)   MEASUREMENT(  1)   ASSERTION(  2)   LOGIC(& )

DIAGNOSIS   :  16
TEST( 46)   STIMULUS( 18)   MEASUREMENT(  1)   ASSERTION(  2)   LOGIC(& )

DIAGNOSIS   :  17
TEST( 31)   STIMULUS( 13)   MEASUREMENT(  1)   ASSERTION(  1)   LOGIC(& )
TEST( 44)   STIMULUS( 17)   MEASUREMENT(  1)   ASSERTION(  3)   LOGIC(& )

DIAGNOSIS   :  18
TEST( 43)   STIMULUS( 17)   MEASUREMENT(  1)   ASSERTION(  2)   LOGIC(& )

DIAGNOSIS   :  19
TEST( 31)   STIMULUS( 13)   MEASUREMENT(  1)   ASSERTION(  1)   LOGIC(& )
TEST( 52)   STIMULUS( 20)   MEASUREMENT(  1)   ASSERTION(  3)   LOGIC(& )

DIAGNOSIS   :  20
TEST( 59)   STIMULUS( 21)   MEASUREMENT(  3)   ASSERTION(  2)   LOGIC(& )
TEST( 32)   STIMULUS( 13)   MEASUREMENT(  1)   ASSERTION(  2)   LOGIC(& )

DIAGNOSIS   :  21
TEST( 33)   STIMULUS( 13)   MEASUREMENT(  1)   ASSERTION(  3)   LOGIC(& )
TEST( 44)   STIMULUS( 17)   MEASUREMENT(  1)   ASSERTION(  3)   LOGIC(& )

DIAGNOSIS   :  22
TEST( 33)   STIMULUS( 13)   MEASUREMENT(  1)   ASSERTION(  3)   LOGIC(& )
TEST( 42)   STIMULUS( 17)   MEASUREMENT(  1)   ASSERTION(  1)   LOGIC(& )

DIAGNOSIS   :  23
TEST( 31)   STIMULUS( 13)   MEASUREMENT(  1)   ASSERTION(  1)   LOGIC(& )
TEST( 83)   STIMULUS( 26)   MEASUREMENT(  1)   ASSERTION(  2)   LOGIC(& )

DIAGNOSIS   :  24
TEST( 84)   STIMULUS( 26)   MEASUREMENT(  1)   ASSERTION(  3)   LOGIC(& )

DIAGNOSIS   :  25
TEST( 24)   STIMULUS( 10)   MEASUREMENT(  1)   ASSERTION(  2)   LOGIC(& )
TEST( 83)   STIMULUS( 26)   MEASUREMENT(  1)   ASSERTION(  2)   LOGIC(& )

DIAGNOSIS   :  26
TEST( 23)   STIMULUS( 10)   MEASUREMENT(  1)   ASSERTION(  1)   LOGIC(& )
TEST( 32)   STIMULUS( 13)   MEASUREMENT(  1)   ASSERTION(  2)   LOGIC(& )
TEST( 83)   STIMULUS( 26)   MEASUREMENT(  1)   ASSERTION(  2)   LOGIC(& )

DIAGNOSIS   :  27
TEST( 58)   STIMULUS( 21)   MEASUREMENT(  3)   ASSERTION(  1)   LOGIC(& )
TEST( 24)   STIMULUS( 10)   MEASUREMENT(  1)   ASSERTION(  2)   LOGIC(& )
TEST( 31)   STIMULUS( 13)   MEASUREMENT(  1)   ASSERTION(  1)   LOGIC(& )
TEST( 39)   STIMULUS( 16)   MEASUREMENT(  1)   ASSERTION(  1)   LOGIC(& )

TOTAL NUMBER OF TEST SETUPS          :  13
TOTAL NUMBER OF ASSERTIONS           :  37
SHORTEST TEST SETUP                  :   1
LONGEST TEST SETUP                   :   9
SHORTEST CONJUNCTION                 :   1
```

Table 4.9 A2100 Logic Optimization Report (continued)

4.4 NOPAL Test Specifications

The most important and final output generated by the top-part of the system is the NOPAL test specification report. Thi report contains all the necessary information to generate an ATLAS program which effectively performs the selected tests and decides on the proper diagnoses. Figure 4.8 shows the NOPAL test specification for the filter subcircuit. The first 12 lines are directives to the code generation.

The first test specified uses an ohmmeter to make a resist measurement. The high side of the meter is connected to termin and the low side is connected to terminal 3 on the printed circ card. The resistance measured is stored in variable RA21_2_1. When the unit is working properly, it is expected to measure minimum 320 Kohm. The maximum measurement could be very high. The ohmmeter is programmed to use 2.8 volt (2800 mV) dc referen voltage source. The assertion requires that the nominal resist be greater than 319 Kohm. If the assertion is true, the nomin diagnosis is selected with a conjunction. If it is not, nothin is done. This situation is processed in another test module.

Test 2 refers to the resistance measurement which was made in Test 1. If the resistance measured is less than 319 Ko diagnosis 4 is selected; which in turn indicates that capacitor C2102 has shorted.

Test 6 makes a complex impedance measurement across termin 3 and 2. The magnitude of the impedance measured is available in variable ZA21_3_6. Minimum expected impedance is 170 ohms, the maximum is 390 ohms. 1 volt rms ac standard signal source used as reference. The impedance measurement is conducted at 1K hertz. If the impedance is 280+-109 ohms, then nominal

```
 /• NOPAL TEST SPECIFICATION SOURCE INPUT, FILE: SAPL1ST */
iL PROCESSOR OPTIONS SPECIFIED: SAPLIST,NOXRcFi,CO0E,SEQ*£,NCXREF2,NOSOURCE2,TRACE=4,De
r NO.

        /**************************************************************************
        /
        /*        NOPAL TEST SPECIFICATION GENERATED BY VERSIOh 1.2 (OCTOBER 79)      *t
        /•                 AUTCMATED TEST DESIGN FOR ANALOG CIRCUITS                  *i
        /•                       DATE   12/19/79    TIMfc   17.42.22                  *i
        /

 1       NOPAL SPECIFICATION   A21C0          ;
        /**************************************************************************
 2        TEST      1 ; /• ISN  *  (   3,   It   1i   1) •/
 3        MEASUREMENT    1(   1) ;
 4          CO*,J : < A 21_ 2    t Ai1.3   > *
 4          OH*KETER< RA21.2.1 CHK, 3.2EC5, 1.2£5fc, 2SCC) TARt: RA21^2.1 ;
 5          ASSERT: R^21 _2~1  > 3.19000E05 ;
 6        LCGIC <   1):    &   1 ;
        y*************************************************************************
 7        TEST      2 ; /• XSN  *  <   4,   2f   1,   2)  */
 8        ^EASL'REMENT    2<   2) ;
 9          AiSERT: RA21_/ 1  < 3.19C0CE05;
10        LOGIC (   23:   ~&   4 ;
        /*************************************************************************
11        TEST      3 ; /* 1SN  s  (  12f   7f   1,   1)  */
12        MEASUREMENT    3(   2) ;
13          CUNJ: < A21 3    , A21 1   > =
13          OH*KET5R< f?A21^3.2 (iHMf 4.5EC2* 7.5E02, 28CC) TARC: RA21.3.3 ;
14          ASSERT: R*21^i33 • 6.C1QCC5C2 •- 1.53CCGEC2 ;
15        LCGIC (   2 ]:    &   1 , & 2 ;
        /*************************************************************************
16        TEST      4 ; /* ISN  5  (  13,   7t   1f   2)  */
17        MEASUREMENT    4(   4) ;
18          ASCLRT: RA21.3.3  < 4.4?0O0EO2;
19        LQGK (   4):    &   t ;
        /*************************************************************************
20        TEST      5 ; /* 1SN  =  <  14f   7f   1,   3)  */
21        MEASUREMENT    5 ( 5 ) ;
22          ASSERT: R;21_3_3  > 7.54G00E02;
23        LOGIC (   5):    &   4 , &   5 ;
        /*************************************************************************
24        TEST      6 ; /* ISN  =  (  15»   &•   1f   1)  */
25        MEASUREMENT    6(   6) ;
26          CUNJ: < A21 3    , A21 2   > =
26          ZMETER( ZA?T_3_6 CHfc, *C.17F02• 0.39EQ3* 1OOC, 100C ) TARG: 2A21_3.6 ;
27          ASSERT: Z*21_i_6  * ;.&1C0CE02 •- 1.C9000E0* ;
28        LCGiC t   e):   *6   1 , & 5 ;
        /*************************************************************************
29        TEST      7 ; /* IS* *  (  17,   6,   1,   3)  +t
30        MEASUREMENT    71   7) ;
31          ASSIST: 2>?1_3_6  > 3.VCGOOE02 ;
32        LGGICC   7):   ~fc   / % /   3;
        /*************************************************************************
```

Figure 4.8 NOPAL Test Specification for A2100 Filter Subscircuit

```
      /*                                                                    *
      /*                  UUT COMPONENT FAILURE DICTIONARY                  *
      /*                                                                    *
      /*********************************************************************
33    COMP_FAIL    1: ALL_COMPS   , FAILURE=NOMINAL     , INDEX=  0 ;
34    COMP_FAIL    2: R2101       , FAILURE=OPEN        , INDEX=  0 ;
35    COMP_FAIL    4: C2101       , FAILURE=OPEN        , INDEX=  0 ;
36    COMP_FAIL    5: C2101       , FAILURE=SHORT       , INDEX=  0 ;
37    COMP_FAIL    6: QDR2101     , FAILURE=OPEN        , INDEX=  0 ;
38    COMP_FAIL    7: QDR2101     , FAILURE=SHORT       , INDEX=  0 ;
      /*********************************************************************
      /*                                                                    *
      /*                  DIAGNOSES AND SPECIAL MESSAGES                    *
      /*                                                                    *
      /*********************************************************************
39     DIAGNOSIS    1:
39       OPERATOR MESSAGE:
39     AFFECTED COMPONENTS =
39            NOMINAL(ALL_COMPS)  ,
39     PRINT= GOOD_UUT ;
40     DIAGNOSIS    2:
40       OPERATOR MESSAGE:
40     AFFECTED COMPONENTS =
40            OPEN(R2101)   ,
40     PRINT= CONJUNCTION ;
41     DIAGNOSIS    3:
41       OPERATOR MESSAGE:
41     AFFECTED COMPONENTS =
41            OPEN(C2101)   ,
41     PRINT= CONJUNCTION ;
42     DIAGNOSIS    4:
42       OPERATOR MESSAGE:
42     AFFECTED COMPONENTS =
42            SHORT(C2101)   ,
42     PRINT= CONJUNCTION ;
43     DIAGNOSIS    5:
43       OPERATOR MESSAGE:
43     AFFECTED COMPONENTS =
43            OPEN(QDR2101)   ,
43     PRINT= CONJUNCTION ;
44     DIAGNOSIS    6:
44       OPERATOR MESSAGE:
44     AFFECTED COMPONENTS =
44            SHORT(QDR2101)   ,
44     PRINT= CONJUNCTION ;
45     DIAGNOSIS    7:
45       OPERATOR MESSAGE:
45     PRINT= BAD_UUT ;
      /*********************************************************************
46     MESSAGE CONJUNCTION:
46             TEXT='POSSIBLE FAULTY COMPONENT(S) ---','(()' ;
47     MESSAGE NODIAGNOSIS:
47             TEXT='FOLLOWING FAILURES (INCLUDING NOMINAL CASE)',
47                  ' WERE NOT DIAGNOSABLE ---','(C)' ;
```

Figure 4.8 NOPAL Test Specification for A2100 Filter Subcircu (continued)

```
4S        PESSfiliE  GOG£_UUT:
48                 TEXT*"**** GOOD UUT ****** ;
49         MESSAGE  BAD  UUT:
49                   TEJT*'**** BAD  UUT  *****   ;
       /***************************************************    ********   **********
       /*
       /•                        UUT  AND  ATE  FUNCTIONS
       /•
       /•*******•******••*****•*•*********•**•**•***•****•*<***  ***_****•*•********
50     FUNCTION:  NOMNAL       t   TYPE  =  ft  PAR AfT -< COMP tS  REAL)  ;
51     FUNCTION :  OP £N        ,   TYPE  *  f,  PARAM =(COMP ,S  REAL)  ;
52     FUNCTION:  SHCRT         ,   TYPE  F,  PA RAM* < COMP ,S  READ  ;
53     FUNCTION:  OHI*METER ,  FUNCTION  TYPE  ' M, -PINS  *  2,
53             PAKAP_1  *  (RESISTANCE,  T  REAL,  LIMIT  *  (OHM,  1CE6*  O>)»
53             PARAP*2  «  (MN.RtS,  S  REAL,  LIMIT  =  (Oh*,  1CEtf,  O),
53             PARAJ*2-  *  CPAX^RcS,  S  REAL,  LIKIT  s  (OhK,  10fc£,  C)>,
53             P4RA.*%  *  <R£F~VCLT,  S  RIAL,  Li^IT  *  (fcVOLT,  tu£3,  -10£3>),
53             COrtFgNITS  a  'AUTOkANGING  OHMMETER*;
54     FINC TICN:  VOLTMSTER ,  FLNCT1ON  TYPE  =  ^,  'rPINS  »  2,
54             PARA^^I  *  (VCLTAbE,  T  REALt  LIKIT  -  (VGLT,  2C0,  -200)),
54             COKMINTS  s  'AUTOHANG1NG  VOLTMETER,  WIDTH  U6,7M$EC,  10Q0  SAPPtES';
55     FUNCTION:  AMFMETcR ,  FUNCTION  7YPc  *  rt,  ~PIN$  *  2,
55             PA»A*_1  «  (CIRKENT,  T  REAL,  LIMIT  *  (AMP,  9,  -9)),
55             COMM^TTS  «  "CURRtNT  ThROtiGH  THE  PObER  SUPPL Y — ES UPPLT";
56     FUNCTION:  ZMCTER ,  FUNCTION  TYPE  *  M,  *PINS  *  2.
56             PARA^.1  -  (C^PLXwIMP,  T  REAL,  LIMIT  *  (CHW,  10E3,  0)),
S6             PAftA»32  s  (F]N.I^P»  S  REAL,  LIMIT  =  <Oh!%  1Ccd,  C)),
56             PARAf^  s  ("AX^IHP,  S  REAL,  LIMIT  «  (Oh^,  1C^6,  C))»
56             PARAI-%  s  (PtF^VCLT,  S  REAL,  LI*1T  *  (VOLT,  7,  O)),
56             PARA!>*5  =  (FHE<.UCN?CY,  S  REAL,  LIMIT  *  (HZ,  12E2,  10)),
56             COM^EfITS  =  'AUTOftANGING  COMPLEX  IMPEDANCE  -  FAGN1TU0S  METER';
57     FUNCTION:  ESIPPLY,  FUNCTION  TYPE  =  S,  ^PINS  *  ^,
57             PARAf-^1  s  (VCLTAbf,  S  REAL,  LIKIT  =  (VCLT,  /t,  0)),
57             PAKA^2^  s  CIlsT_StS,  S  REAL»  LIMIT  -  (OHM,  4,  Q)),
57             COMKcNTS  *  '@hch  SUPPLY  —OC?A,  MAX  9AMP,  1 ^T.BR ES  IGNORED*;
       /4«'**4tr«'*#«**-**«**4«*-**<ir«ik4****«4*******«******4****   «*•**«*****************<<
       ^*
       /.*                       UUT  TEST  TERMINALS
       /*
       /***-**-**********.*•     ft*********_************      •>*****************************
58     UUT^POIN'T:  Ac1^3        9  CONNECTORS  JS            )  ;
                   /*  G^OUNO
59     UUT _POINT:  A 21  X       ,  CCNNECTOR=(  J8            >  ;
                   / • J^
60     UUT_PCINT:  A^1.2         >  CONNECTO«=s(  J8            )  ;
       /ft*************************  *************************  4***  ****************

       /*                   ENO  CF  NOPAL  TFST  SPECIFICATIONS
       /*
       /«***««******«*******«*******««**«*ft*************************************i
d1     ENOA710C         ;
cPROR/WAR SING  MESSAGES  GENERATED              DURING NOPAL  SYNlAX  ANALYSIS:
•STATISTICS* NO. OF SAP ERRORS *    0   ,   HO. OF WARNINGS =    0   , NO* OF STATEMEf
```

Figure 4.8 NOPAL Test Specification for A2100 Filter Subcircuit (continued)

agnosis is selected. If a higher than 390 ohms is measured
ther capacitor C2101 or resistor R2101 could be open.

Following the test modules, UUT components and their failure
nctions are listed. Failure number 3 (short of R2101) is
itted since this class of failures were considered unlikely
d dropped from analysis. The diagnoses identify the affected
mponents and issue a message when they are selected.

The UUT and ATE functions define and describe the function
d their parameters. These functions were described in Section 3.3

The NOPAL test specification for the voltage regulator and
me delay circuit is similar to the specification described
ove. It is not listed in this report due to its length. A
py of the listing is available on the accompanying computer tape.

4.5 ATLAS Program

The bottom part of the NOPAL system generates ATLAS progra from NOPAL specification. Figure 4.9 is an ATLAS compiler list of a program used to test the filter subcircuit. In the beginn of the program, test module, diagnosis, and affected component names are uniquely identified with an index. Then, a number of system variables and constants are declared. A disk file named "UPCX21" (included during compilation) contains the actual DIU pin assignments to the test point names used in the NOPAL speci cation. Another disk file named "UPFLBS" (also included during compilation) contains the ATLAS function library of all the fun used in the specification. "AFF-COMP.PRINT" is a utility proce which points the failure name of a component for given subscrip "UPFIP" is another disk file which contains utility procedures keep track of the fault isolation state. These procedures are not essential to the execution logic of the program. They mere provide a fault isolation status summary upon program terminati

Each diagnosis in the NOPAL specification becomes a diagno procedure in the ATLAS program. In the beginning of the proced there is a check to determine whether or not the diagnosis is actually selected. This check is done only for those diagnoses which are selected by conjunctions. If it is a diagnosis selec unconditionally or by disjunction, this code is omitted. Then there are a few lines of code which keep track of the affected components. Finally the text of the message to operator is iss This code is omitted if there is no message in the diagnosis.

Each test module in the NOPAL specification becomes an ATI test procedure. First, a number of system flags are set. Then

```
 1:         BEGIN EQUATE PROGRAM 'A2100-SMALL' $
 2: C          NAMES                    INDEX
 3: C           *** TEST MODULES ***
 4: C           'TEST.9'            --   1
 5: C           'TEST.10'           --   2
 6: C           'TEST.11'           --   3
 7: C           'TEST.12'           --   4
 8: C           'TEST.13'           --   5
 9: C           'TEST.14'           --   6
10: C           'TEST.15'           --   7
11: C
12: C           *** DIAGNOSES ***
13: C           'DIAG.1'            --   1
14: C           'DIAG.4'            --   2
15: C           'DIAG.6'            --   3
16: C           'DIAG.2'            --   4
17: C           'DIAG.5'            --   5
18: C           'DIAG.3'            --   6
19: C           'DIAG.7'            --   7
20: C
21: C           *** AFFECTED COMPONENTS ***
22: C            SHORT(QDR2101)              --   1
23: C            OPEN(QDR2101)               --   2
24: C            SHORT(C2101)                --   3
25: C            OPEN(C2101)                 --   4
26: C            SHORT(R2101)                --   5
27: C            OPEN(R2101)                 --   6
28: C            NOMINAL(ALL-COMPS)          --   7
29: C      $
30: C     DECLARATIONS OF SYSTEM VARIABLES  $
31:          DECLARE DIGITAL, LIST,'SYS.DIAG-FLAG'(7) $
32:          DECLARE DECIMAL, 'SYS.S-TIME' $
33:          DECLARE DECIMAL, 'SYS.D-TIME' $
34:          DECLARE DECIMAL, 'SYS.DUMMY' $
35:          DECLARE DECIMAL, 'SYS.NAME' $
36:          DECLARE DECIMAL, LIST,'SYS.#TESTS IN CONJ'(7) $
37:          DECLARE DIGITAL, LIST, 'SYS.TEST-FLAG'(7) $
38:          DECLARE DIGITAL, 'SYS.FLAG' $
39:          DECLARE DIGITAL, 'SYS.ASRT-FLAG' $
40:          DECLARE DECIMAL, 'SYS.TIM', 'SYS.TIME' $
41:          DECLARE DECIMAL, LIST, 'SYS.CLOCK'(6)  $
42:          DECLARE DECIMAL, 'SYS.I' $
43:          DECLARE DIGITAL, 'SYS.Y/N' $
44:          DECLARE DIGITAL, 'SYS.STATE' $
45:          DECLARE DIGITAL, 'SYS.SELECT' $
46:          DECLARE DECIMAL, LIST, 'AFF-COMP.NAME'(1) $
47:          DECLARE DIGITAL, LIST, 'AFF-COMP.SELECT'(1) $
48:          DECLARE DECIMAL, LIST, 'AFF-COMP.WHERE'(7) $
49:          DECLARE DIGITAL, LIST, 'AFF-COMP.STATE'(7) $
50:          DECLARE DECIMAL, 'AFF-COMP.TEST' $
51:          DECLARE DECIMAL, 'AFF-COMP.COUNT' $
52:          DECLARE DIGITAL, 'AFF-COMP.CHANGE' $
53: C     *** CONSTANTS ***  $
54:          DEFINE 'SYS.SELECTED' , B'10' $
55:          DEFINE 'SYS.NOT SELECTED' , B'01' $
56:          DEFINE 'SYS.NOT TESTED' , B'00' $
57:          DEFINE 'SYS.TESTED' , B'10' $
58:          DEFINE 'SYS.SKIPPED' , B'01' $
59:          DEFINE 'SYS.#DIAGS' , 7 $
60:          DEFINE 'SYS.#TESTS' , 7 $
```

Figure 4.9 ATLAS For A2100 Filter

```
61:          DEFINE 'SYS..TRUE' , B'1' S
62:          DEFINE 'SYS..FALSE' , B'O' %
63:          DEFINE 'SYS..OONT KNOW, B'OO' ^
64:          OFF IME 'SYS..IS',B'rt01L#s
65:          DEFINE 'SYS..IS «MOT', o#010# «
66:          OEFIVE 'SYS..MAY 9E', *'O1t' «
67:          DFFtME 'SYS.,MAY RF MOT', PMOO' 5
68:          DEFTNF 'SYS^COMPONEMTS',7 5
69: C    UL.IT POINT DEFINITIONS $
70: C    FOLLOWING DISK FILE SHOULD CONTAIN THE
71: C    MISSING EQUATE/UUT Pitt * Oly ASSIGNMENTS* $
72:          INCLUOE "UPCX21" S
73: C     A2100 'JUT CONNECTIONS S
74:       f^(Tf?TNfC 'A21-1',, 525
75:       nfs*tr I^P* 'A21-?',- 515
76:       DEFINE 'A21-3'ir ^OS
77:       OEFIN'F 'A2i-a',, 595
78:       DEFINE 'A21-5',. 61$
79:       DEFINE '421-*.',, *>3S
80:       DEFINE 'A21-7',, ?5s
81:       DSFIME 'A21-8',, 515
82:       DEFINE 'A21-"'(r 315
83: C     OFFIMf '5N0',  MS  C FOP THE Mi IN CIPC'JIT S
84: C     DEFINE 'GNO',  505  C FOP THE SMALL CIRCUIT $
85: C    MAC«?O DEFINITIONS $
86:          DEFINE 'PRT,.TIME', 'SYS.CLOCK'CD , • «*:",
87:                'SYS.CLOCK'(2), "##:", 'SYS.CLOCK'(3), "##" S
88: C    DECLARATIONS FOR USFR DEFINED GLOPAL VAPIABLES S
89:          OECLAPE DECIMAL, '9*21-3-9' S
90:          OECLAPE DECIMAL, '9A21-3-11' $
91:          OECLAPE DECIMAL, 'ZA21-3-14' $
92: C    SYSTEM UTILITY ROUTINES S
93:          DEFTNE PROCEDURE, 'GET.TI^E' S
94:            PEADCTI^E 'SYS.CLOC^'CD ALL), SYS-CLOCK 5
95:            'SYS.TI«E' s 3600*'SYS#CLOCK'fn + 60*'SYS.CLOC^'f2)
96:                'SYS.CLOCK'(3) S
97:          END 'SET.TIME' S
98:          DECLARF DECIMAL, 'SYS#DEC.O1' «
99:          DECLARE DECIMAL, 'SVS#DFC.O2' S
00: C S
01: C    USER PEFIMED ATE FUNCTIONS $
02: C S
03:          INCLUDE "UPFL^S11 $
04:  OEFINE  PPOCEDURE, 'OHMMETEP'S
05:      DECLARE OECIMAL, '0HMMETFP.PRM01',
06:          '0HMMET£R#PRM02','OHMMETEP•PP^03','OHMMpTEP#PRM0a ',
07:      -   'OHMMETER.RES', 'OHMMETEP#MAX', *r»HMMPTFR#LL ', 'OHMMFTEP.IU
08:          #QWMMPTFR#LAST', 'OHMMETFR#COUNT', 'OMMMCTCPmLP j •9#nMMMETi;
09:          'OHMMETEP.CNX01','OHMMETEP.CNvQ?*S
10:      DECLARE DECIMAL, LIST, 'QHMMgTEP.PNS'(5) 5
11:     'OHMMETER.RNG'(1) = 0 $
12:     'OHMM?TFR#PMG'C2) s 3999   S  'OHMMETER.RNS'f3) * 39999 $
13:     'OHMMETER.RNG'(4) = 399999 5  'OHMMETER.RNG'(5) = 1E6 $
14:     •OHMMETFR.LAST' s •! 5
15: 10  'OH«*METEP«COUMT' s 0 S
16:      COMPARE 'OHMMETEP.PRMO^'f LT 4000 $  GOTO STFP 11 IF MQGO 5
17:            •OHMMETEP.LRI' * 2 « GOTO STrp ]a %
18: It   COMPARE 'OHMMPTEP.PRMO?', LT 40000 S  GOTO STEP 12 IF MOGO S
19:            •OHMMPTFP.LPT' s 3 S GOTO STEP 1^ $
20: 12   COMPAPF *OHMMET?P#OP^OP_B. LT annnnn ^  GOTO STEP 13 IF MOGO
```

```
l:          'OHMMETER.LRI' = 4 $ GOTO STEP 14 $
2: 13       'OHMMETER.LRI' = 5 $
3: 14   COMPARE 'OHMMETER.PRM03', LT 4000 $  GOTO STEP  15 IF NOGO $
l:          'OHMMETER.URI' = 2 $ GOTO STEP 18 $
5: 15   COMPARE 'OHMMETER.PRM03', LT 40000 $  GOTO STEP 16 IF NOGO $
:           'OHMMETER.URI' = 3 $ GOTO STEP 18 $
': 16   COMPARE 'OHMMETER.PRM03', LT 400000 $  GOTO STEP 17 IF NOGO $
l:          'OHMMETER.URI' = 4 $ GOTO STEP 18 $
): 17       'OHMMETER.URI' = 5 $
): 18   'OHMMETER.MAX' = 'OHMMETER.RNG'('OHMMETER.LRI') $
:        COMPARE 'OHMMETER.CNX01' + 'OHMMETER.CNX02', LE 200 $
2:          GOTO STEP 19 IF GO $
3:        DISPLAY "PROBE HI ", 'OHMMETER.CNX01', "### LO ", 'OHMMETER.
l:       MONITOR (RES 'OHMMETER.PRM01' OHM),IMPEDANCE,
5:            REF-VOLTAGE 'OHMMETER.PRM04' MV, RES MAX 'OHMMETER.MAX'
:             CNX PROBE $
':       'OHMMETER.COUNT' = 1 $
l:       GOTO STEP 21 $
): 19    INITIATE (RES 'OHMMETER.PRM01' OHM),IMPEDANCE,
l:            REF-VOLTAGE 'OHMMETER.PRM04' MV, RES MAX 'OHMMETER.MAX'
:             CNX HI 'OHMMETER.CNX01' LO 'OHMMETER.CNX02'$
!: 20   READ (RES 'OHMMETER.PRM01' OHM), IMPEDANCE $
l:     'OHMMETER.COUNT' = 'OHMMETER.COUNT' + 1 $
l:      COMPARE 'OHMMETER.PRM01', GT 10E6$ GOTO STEP 21 IF GO $
i:      COMPARE ABS(('OHMMETER.PRM01'-'OHMMETER.LAST')/'OHMMETER.PRM01
:      'OHMMETER.LAST'='OHMMETER.PRM01'$  GOTO STEP 20 IF NOGO$
': 21   RECORD 'AFF-COMP.TEST',"TEST ##: ",'OHMMETER.PRM01'/1E3,
l:        "######.### KOHM, ",'OHMMETER.PRM04',"#### MV, ",
l:        ('OHMMETER.MAX'+1)/1E3, "#### KOHM, ",'OHMMETER.COUNT'," ##
l:        "CNX(",'OHMMETER.CNX01',"##,",'OHMMETER.CNX02',"##)"$
:       COMPARE 'OHMMETER.PRM01',
!:            UL 'OHMMETER.RNG'('OHMMETER.LRI') $  GOTO STEP 22 IF GO
i:     'OHMMETER.LRI' = 'OHMMETER.LRI' +1 $
l:      COMPARE 'OHMMETER.LRI', GT 'OHMMETER.URI' + 0.5 $ GOTO STEP 18
i: 22   REMOVE DC-STD $
:       END 'OHMMETER'$
': C*************************************************************************
:  DEFINE  PROCEDURE, 'ZMETER'$
l:      DECLARE DECIMAL, 'ZMETER.PRM01',
:             'ZMETER.PRM02','ZMETER.PRM03','ZMETER.PRM04','ZMETER.PRM05
:             'ZMETER.RES','ZMETER.MAX','ZMETER.LL','ZMETER.UL',
:             'ZMETER.LAST','ZMETER.COUNT','ZMETER.LRI','ZMETER.URI',
:             'ZMETER.CNX01','ZMETER.CNX02'$
:      DECLARE DECIMAL, LIST, 'ZMETER.ARG'(3),'ZMETER.RNG'(5) $
:     'ZMETER.RNG'(1) = 0 $
:     'ZMETER.RNG'(2) = 3600    $  'ZMETER.RNG'(3) = 36000 $
:     'ZMETER.RNG'(4) = 360000 $  'ZMETER.RNG'(5) =  1E6 $
:     'ZMETER.LAST' = -1 $
: 30 'ZMETER.COUNT' = 0 $
:      COMPARE 'ZMETER.PRM02', LE 3600 $  GOTO STEP  31 IF NOGO $
:            'ZMETER.LRI' = 2 $ GOTO STEP 34 $
: 31   COMPARE 'ZMETER.PRM02', LE 36000 $  GOTO STEP 32 IF NOGO $
:            'ZMETER.LRI' = 3 $ GOTO STEP 34 $
: 32   COMPARE 'ZMETER.PRM02', LE 360000 $  GOTO STEP 33 IF NOGO $
:            'ZMETER.LRI' = 4 $ GOTO STEP 34 $
: 33         'ZMETER.LRI' = 5 $
: 34   COMPARE 'ZMETER.PRM03', LE 3600 $  GOTO STEP  35 IF NOGO $
:            'ZMETER.URI' = 2 $ GOTO STEP 38 $
: 35   COMPARE 'ZMETER.PRM03', LE 36000 $  GOTO STEP 36 IF NOGO $
:            'ZMETER.URI' = 3 $ GOTO STEP 38 $
```

```
36  COMPARE #ZVETEP.PPM03', LE 3*0000 «  GOTO *TF» ?7 IF MHGD *
          'ZMETER.URI' s a S GOTO STFP 3* ?
37        '7M£TE*.iJPI' = 5 n
33 'ZMETER.M4X' * 'Z"ETE*.PMG'C'ZMETFP.LRI') <5
   COMPARE 'ZMETFP#C*X01' * *ZMETES.C\»X02', LE 200 $
      GOTO STE° 3<* IF GO S
      DISPLAY "PROBE HI ", '7METER.CMX01', "*** LO ", 'ZM£T£P.CNX03(
  MONITOR fIMP #7MPTEP,APG# f!) OMM-DEG-H75,IMPpoAMCE#FPEO #ZV£TEP.P«
         PEF-VOLTAGE #ZMETER#PPM04# MV# IMP MAy #7MFTER#MA*' HHM,
         CVX HT #ZMETEP.CNX01' LO #ZMFT£P.C^XO? V?
   'ZMETEP.COUNT' 2 1 $
    ^OTO STE° ai 5
39 INTTTATECIMP #£METEP.APG*(1) OHM-OFS-HZ),TMPEDANCF#FREO '7MPTEP.P
         °EF-VOLTAGE 'ZMFTE'.PP^Oa' Mv, IMP MAX #ZMST£»#MAX# OH",
         CNX HI #7M£TER.CW01# LO 'Z^ETFP#CMvr»?•5
ao  PEAO CTMP. #ZM£TEP.APG*f1) OHM-OEG-HZ), IMPEDANCES
   'ZMETER.PPM01# s *ZMETEP#4PG# f1) •«
   'ZMETER.COUNT' s #ZM£TEP#COUMT# • 1 S
    COMPARE 'ZMETER.PPM01#, GT 10E6S GOTO STFP ai IF GO S
    cf)MPARP A8^(t*7METER#PPM01'-'ZMf-TEP.LAST')/'7METEP.PSMO1#)# LE 1
   #ZMETER,LAST#s'ZMETEP.PPMCl'S  GOTO STEP 40 IF NOGOS
at  PECOPO #AFF-CdMP#TFST#,-TEST **1 ",'Z^ETFR.PPMOI VIF3r
      "##.### KOHM,",'ZMETER.ARG'(2),"### DEG, ",
      'ZMETER.ARG'(3),"#### HZ, ••,'ZMI-TEP.PPMOa',"unuu MV, w,
      f'ZMETER.MAX')/lE3f "#**.* K0HMf w, 'ZMETFP.COUNT#frt «tf TTMES,
      "CMtf"#"7M£tER*CNX01*,»**,*, *Z^ETEP.C^XO?#, "**) "S
    COMPARE #ZMETEP#PRMOt*9
          1IL #ZMPTEP.RMG#f#7METEP*LPI#) «  GOTO STEP a2 IF GO S
   '7METER.LRI' s 'ZM£TER#LPI# >1 S
    COMPARE 'ZM£T£R#LRI'# GT #ZMETEP*UPIV • 0#5 % GOTO STEP 33 IF WO
42  P£M0V£ AC-STD "$
    ENO 'ZMETER'S
C***********************************************************************$
  DEFINE  PROCEDURE,'VOLTMFTER' S
DECLARE  DECIMAL,'VOLTMETER.PRMO1','VOLTMETER.RFS#,
              'VOLTMETER.CMX01','VOLTM£TEP#rMXO2'S
     MEASURE (VOLTAGE 'VOLTMETER.RES' V),
          OC-SIC«MAL#OELAY 0.1 SFC,
          CMX HI 'V0LTMETFR.CMV01'
          LO 'VOLTMETER.CMX02' J
70   MEASURE (VOLTAGE 'VOLTMETER.PRM01' V),
          OC-SIGWAL,DELAY 0.1 SEC,
          C^X HI 'VOLTMETER.CMX01'
          LO 'VOLTMETER.C^XO?' S
 COMPARE ARStC'VOLTMETER.PRM01'-'VOLTMETFR.RES')/'VOLJMETEP.PPMQt#),
          LE 0.00555
 GOTO STEP 70 IF MOGOS
RECOPO 'AFF-COMP.TEST',"TEST **: MEA^UPEO «,'VOLTMETER.PRMO1 •,
       *U9UU* V, CMX HI *,
       'VOLTMETER.CNXO1',»* LO ",'VOLTMFTER.CNXO?*,n* .tt $
 E^O 'VOLTMETER' S
C***********************************************************************$
 DEFINE  PROCEDURE,#ESUPPLY' $
DECLARE DECIMAL,'ESUPPLY.°PM0t','ESUPPLY#PRM02', 'ESUPPLY#RFS',
       'ESUPPLY.CNX01', 'ESUPPLY.CNX02'S
REMOVE 0C2AS
APPLY OC-SIGWAL DC2A,VOLTAGE 'FSUPPLY.PRMQ1' V,
       CMX HI 'ESUPPLY.CNXOt' LO 'ESUPPLY.CWVQ?' S
RECORD 'AFF-COMP.TFST',"TEST *#z APPLIED DC2A, ",
       'ESUPPLY#PRM01O,"Umttn* V* CMX HT •.
```

```
:         'ESUPPLY.CNX01',"# LO ",
:         'ESUPPLY.CNX02',"# ." $
:  MEASURE (CURRENT 'ESUPPLY.RES' A),
:    DC-SIGNAL,DELAY 0.1 SEC,CNX DC2A $
:   RECORD "              MEASURED ",'ESUPPLY.RES',     "#.### AMPS THRU
: END 'ESUPPLY' $
: C*****************************************************************
:          DEFINE PROCEDURE, 'AFF-COMP.PRINT'$
: 300      COMPARE 'SYS.I', LT 2 $ GOTO STEP 305 IF NOGO $
:          RECORD 'AFF-COMP.COUNT',"###: SHORT(QDR2101)"$ GOTO STEP
: 305      COMPARE 'SYS.I', LT 3 $ GOTO STEP 310 IF NOGO $
:          RECORD 'AFF-COMP.COUNT',"###: OPEN(QDR2101)"$ GOTO STEP 3
: 310      COMPARE 'SYS.I', LT 4 $ GOTO STEP 315 IF NOGO $
:          RECORD 'AFF-COMP.COUNT',"###: SHORT(C2101)"$ GOTO STEP 33
: 315      COMPARE 'SYS.I', LT 5 $ GOTO STEP 320 IF NOGO $
:          RECORD 'AFF-COMP.COUNT',"###: OPEN(C2101)"$ GOTO STEP 335
: 320      COMPARE 'SYS.I', LT 6 $ GOTO STEP 325 IF NOGO $
:          RECORD 'AFF-COMP.COUNT',"###: SHORT(R2101)"$ GOTO STEP 33
: 325      COMPARE 'SYS.I', LT 7 $ GOTO STEP 330 IF NOGO $
:          RECORD 'AFF-COMP.COUNT',"###: OPEN(R2101)"$ GOTO STEP 335
: 330      RECORD 'AFF-COMP.COUNT',"###: NOMINAL(ALL-COMPS)"$
: 335      END 'AFF-COMP.PRINT'$
:          INCLUDE "UPFIP" $
: DEFINE PROCEDURE, 'PRINT.DONT KNOW' $
:  RECORD "LIST OF COMPONENTS FOR WHICH NO DIAGNOSIS HAS BEEN MADE:"
:  'AFF-COMP.COUNT' = 0$
:  FOR 'SYS.I' = 1 THRU 'SYS.#COMPONENTS' THEN$
:      COMPARE 'AFF-COMP.STATE'('SYS.I'),EQ 'SYS.DONT KNOW'$
:      GOTO STEP 710 IF NOGO $
:      'AFF-COMP.COUNT' = 'AFF-COMP.COUNT' + 1 $
:      PERFORM 'AFF-COMP.PRINT' $
: 710 END FOR $
: COMPARE 'AFF-COMP.COUNT',GT 0 $
: GOTO STEP 711 IF GO $
: RECORD "*** NONE *** " $
: 711 RECORD "END OF LIST." $
:   END 'PRINT.DONT KNOW' $
: DEFINE PROCEDURE, 'PRINT.MAY BE' $
: RECORD "LIST OF COMPONENTS WHICH MAY BE AFFECTED:"$
:  'AFF-COMP.COUNT' = 0$
:  FOR 'SYS.I' = 1 THRU 'SYS.#COMPONENTS' THEN$
:      COMPARE 'AFF-COMP.STATE'('SYS.I'),EQ 'SYS.MAY BE'$
:      GOTO STEP 720 IF NOGO $
:      'AFF-COMP.COUNT' = 'AFF-COMP.COUNT' + 1 $
:      PERFORM 'AFF-COMP.PRINT' $
: 720 END FOR $
: COMPARE 'AFF-COMP.COUNT',GT 0 $
: GOTO STEP 721 IF GO $
: RECORD "*** NONE *** " $
: 721 RECORD "END OF LIST." $
:   END 'PRINT.MAY BE' $
: DEFINE PROCEDURE, 'PRINT.MAY BE NOT' $
: RECORD "LIST OF COMPONENTS WHICH MAY NOT BE AFFECTED :" $
:  'AFF-COMP.COUNT' = 0$
:  FOR 'SYS.I' = 1 THRU 'SYS.#COMPONENTS' THEN$
:      COMPARE 'AFF-COMP.STATE'('SYS.I'),EQ 'SYS.MAY BE NOT'$
:      GOTO STEP 730 IF NOGO $
:      'AFF-COMP.COUNT' = 'AFF-COMP.COUNT' + 1 $
:      PERFORM 'AFF-COMP.PRINT' $
: 730 END FOR $
```

```
301:  COMPARE 'AFF-COMP.COUNT',GT 0 $
302:  GOTO STEP 731 IF GO $
303:  RECORD "*** NONE *** " $
304: 731 RECORD "END OF LIST." $
305:   END 'PRINT.MAY BE NOT' $
306:  DEFINE PROCEDURE, 'PRINT.IS' $
307:  RECORD "LIST OF COMPONENTS WHICH ARE AFFECTED: " $
308:   'AFF-COMP.COUNT' = 0$
309:   FOR 'SYS.I' = 1 THRU 'SYS.#COMPONENTS' THEN$
310:       COMPARE 'AFF-COMP.STATE'('SYS.I'),EQ 'SYS.IS'$
311:       GOTO STEP 740 IF NOGO $
312:       'AFF-COMP.COUNT' = 'AFF-COMP.COUNT' + 1 $
313:       PERFORM 'AFF-COMP.PRINT' $
314: 740 END FOR $
315:  COMPARE 'AFF-COMP.COUNT',GT 0 $
316:  GOTO STEP 741 IF GO $
317:  RECORD "*** NONE *** " $
318: 741 RECORD "END OF LIST." $
319:   END 'PRINT.IS' $
320:  DEFINE PROCEDURE, 'PRINT.IS NOT' $
321:  RECORD "LIST OF COMPONENTS WHICH ARE NOT AFFECTED :"$
322:   'AFF-COMP.COUNT' = 0$
323:   FOR 'SYS.I' = 1 THRU 'SYS.#COMPONENTS' THEN$
324:       COMPARE 'AFF-COMP.STATE'('SYS.I'),EQ 'SYS.IS NOT'$
325:       GOTO STEP 750 IF NOGO $
326:       'AFF-COMP.COUNT' = 'AFF-COMP.COUNT' + 1 $
327:       PERFORM 'AFF-COMP.PRINT' $
328: 750 END FOR $
329:  COMPARE 'AFF-COMP.COUNT',GT 0 $
330:  GOTO STEP 751 IF GO $
331:  RECORD "*** NONE *** " $
332: 751 RECORD "END OF LIST." $
333:   END 'PRINT.IS NOT' $
334:  DEFINE PROCEDURE, 'AFF-COMP.UPDATE'$
335:        FOR 'SYS.I' = 1 THRU 'AFF-COMP.COUNT' THEN $
336:        'SYS.NAME'='AFF-COMP.NAME'('SYS.I')$
337:        'SYS.STATE'='AFF-COMP.STATE'('SYS.NAME')$
338:        'SYS.SELECT'='AFF-COMP.SELECT'('SYS.I')$
339:     COMPARE 'SYS.STATE', EQ 'SYS.DONT KNOW'$
340:     GOTO STEP 760 IF NOGO$
341:     GOTO STEP 766$
342: 760 COMPARE 'SYS.STATE', EQ 'SYS.IS'$
343:     GOTO STEP 761 IF NOGO$
344:        COMPARE 'SYS.SELECT', EQ 'SYS.IS'$
345:        GOTO STEP 766 IF GO$
346:        COMPARE 'SYS.SELECT', EQ 'SYS.IS NOT'$
347:        GOTO STEP 767 IF GO$
348:        COMPARE 'SYS.SELECT', EQ 'SYS.MAY BE'$
349:        GOTO STEP 768 IF GO$
350:        GOTO STEP 767$
351: 761 COMPARE 'SYS.STATE', EQ 'SYS.IS NOT'$
352:     GOTO STEP 762 IF NOGO$
353:        COMPARE 'SYS.SELECT', EQ 'SYS.IS'$
354:        GOTO STEP 767 IF GO$
355:        COMPARE 'SYS.SELECT', EQ 'SYS.IS NOT'$
356:        GOTO STEP 766 IF GO$
357:        COMPARE 'SYS.SELECT', EQ 'SYS.MAY BE'$
358:        GOTO STEP  767 IF GO$
359:        GOTO STEP 768$
360: 762 COMPARE 'SYS.STATE', EQ 'SYS.MAY BE'$
```

```
1:       GOTO STEP 763 IF NOGOS
2:          COMPARE 'SYS.SELECT', EQ 'SYS.IS'S
3:          GOTO STEP 766 IF GOS
4:          COMPARE 'SYS.SELECT', EQ 'SYS.IS NOT'S
5:          GOTO STEP 764 IF GOS
6:          COMPARE 'SYS.SELECT', EQ 'SYS.MAY BE'S
7:          GOTO STEP  766 IF GOS
8:          GOTO STEP  764S
9: 763 COMPARE 'SYS.STATE', EQ 'SYS.MAY BE NOT'S
0:       GOTO STEP 768 IF NOGOS
1:          COMPARE 'SYS.SELECT', EQ 'SYS.IS'S
2:          GOTO STEP 764 IF GOS
3:          COMPARE 'SYS.SELECT', EQ 'SYS.IS NOT'S
4:          GOTO STEP 766 IF GOS
5:          COMPARE 'SYS.SELECT', EQ 'SYS.MAY BE'S
6:          GOTO STEP  764 IF GOS
7:          GOTO STEP  766S
8: 764  RECORD "*** WARNING: FAULT ISOLATION LOGIC INCONSISTANCY"S
9: 765  RECORD "COMPONENT:", 'SYS.NAME', " ###;"S
0:       RECORD "LAST STATE:", 'SYS.STATE' R 2, " B'####'; ",
1:              "IN TEST:", 'AFF-COMP.WHERE'('SYS.NAME'), " ###; "S
2:      RECORD "CURRENT STATE:", 'SYS.STATE' R 2, " B'####'; ",
3:              "IN TEST:", 'AFF-COMP.TEST', " ### "S
4: 766 'AFF-COMP.STATE'('SYS.NAME')='SYS.SELECT'S
5:      'AFF-COMP.WHERE'('SYS.NAME')='AFF-COMP.TEST'S
6:      GOTO STEP 768 S
7: 767 RECORD "*** ERROR: FAULT ISOLATION LOGIC INCONSISTANCY"S
8:      GOTO STEP 765S
9: 768 END FORS
0:       END 'AFF-COMP.UPDATE'S
1:
2: C*****************************************************************
3: C*****************************************************************
4: C     DIAGNOSES PROCS $
5: C*****************************************************************
6: C*****************************************************************
7:  1000     DEFINE PROCEDURE, 'DIAG.1' $
8:           'SYS.#TESTS IN CONJ'(1) = 'SYS.#TESTS IN CONJ'(1) - 1  $
9:           COMPARE 'SYS.#TESTS IN CONJ'(1), LE 0  $
0:           GOTO STEP  1005       IF NOGO $
1:           'AFF-COMP.COUNT' = 1 $
2:           'AFF-COMP.NAME'(1) = 7 $
3:           'AFF-COMP.SELECT'(1) = 'SYS.MAY BE' $
4:           PERFORM 'AFF-COMP.UPDATE' $
5:           RECORD "**** GOOD UUT ****" $
6:           'SYS.DIAG-FLAG'(1) = 'SYS.SELECTED' $
7:  1005     END 'DIAG.1' $
8: C*****************************************************************
9:  1100     DEFINE PROCEDURE, 'DIAG.4' $
0:           'SYS.#TESTS IN CONJ'(2) = 'SYS.#TESTS IN CONJ'(2) - 1  $
1:           COMPARE 'SYS.#TESTS IN CONJ'(2), LE 0  $
2:           GOTO STEP  1105       IF NOGO $
3:           'AFF-COMP.COUNT' = 1 $
4:           'AFF-COMP.NAME'(1) = 3 $
5:           'AFF-COMP.SELECT'(1) = 'SYS.MAY BE' $
6:           PERFORM 'AFF-COMP.UPDATE' $
7:           RECORD "POSSIBLE FAULTY COMPONENT(S) ---!LSHORT(C2101)  "
8:           'SYS.DIAG-FLAG'(2) = 'SYS.SELECTED' $
9:  1105     END 'DIAG.4' $
0: C*****************************************************************
```

```
 1200    DEFINE PROCEDURE, 'DIAG.6' $
         'SYS.#TESTS IN CONJ'(3) = 'SYS.#TESTS IN CONJ'(3) - 1  $
         COMPARE 'SYS.#TESTS IN CONJ'(3), LE 0  $
         GOTO STEP  1205      IF NOGO $
         'AFF-COMP.COUNT' = 1 $
         'AFF-COMP.NAME'(1) = 1 $
         'AFF-COMP.SELECT'(1) = 'SYS.MAY BE' $
         PERFORM 'AFF-COMP.UPDATE' $
         RECORD "POSSIBLE FAULTY COMPONENT(S) ---!LSHORT(QDR2101)  "
         'SYS.DIAG-FLAG'(3) = 'SYS.SELECTED' $
 1205    END 'DIAG.6' $
C**********************************************************************
 1300    DEFINE PROCEDURE, 'DIAG.2' $
         'SYS.#TESTS IN CONJ'(4) = 'SYS.#TESTS IN CONJ'(4) - 1  $
         COMPARE 'SYS.#TESTS IN CONJ'(4), LE 0  $
         GOTO STEP  1305      IF NOGO $
         'AFF-COMP.COUNT' = 1 $
         'AFF-COMP.NAME'(1) = 6 $
         'AFF-COMP.SELECT'(1) = 'SYS.MAY BE' $
         PERFORM 'AFF-COMP.UPDATE' $
         RECORD "POSSIBLE FAULTY COMPONENT(S) ---!LOPEN(R2101)  " $
         'SYS.DIAG-FLAG'(4) = 'SYS.SELECTED' $
 1305    END 'DIAG.2' $
C**********************************************************************
 1400    DEFINE PROCEDURE, 'DIAG.5' $
         'SYS.#TESTS IN CONJ'(5) = 'SYS.#TESTS IN CONJ'(5) - 1  $
         COMPARE 'SYS.#TESTS IN CONJ'(5), LE 0  $
         GOTO STEP  1405      IF NOGO $
         'AFF-COMP.COUNT' = 1 $
         'AFF-COMP.NAME'(1) = 2 $
         'AFF-COMP.SELECT'(1) = 'SYS.MAY BE' $
         PERFORM 'AFF-COMP.UPDATE' $
         RECORD "POSSIBLE FAULTY COMPONENT(S) ---!LOPEN(QDR2101)  " $
         'SYS.DIAG-FLAG'(5) = 'SYS.SELECTED' $
 1405    END 'DIAG.5' $
C**********************************************************************
 1500    DEFINE PROCEDURE, 'DIAG.3' $
         'SYS.#TESTS IN CONJ'(6) = 'SYS.#TESTS IN CONJ'(6) - 1  $
         COMPARE 'SYS.#TESTS IN CONJ'(6), LE 0  $
         GOTO STEP  1505      IF NOGO $
         'AFF-COMP.COUNT' = 1 $
         'AFF-COMP.NAME'(1) = 4 $
         'AFF-COMP.SELECT'(1) = 'SYS.MAY BE' $
         PERFORM 'AFF-COMP.UPDATE' $
         RECORD "POSSIBLE FAULTY COMPONENT(S) ---!LOPEN(C2101)  " $
         'SYS.DIAG-FLAG'(6) = 'SYS.SELECTED' $
 1505    END 'DIAG.3' $
C**********************************************************************
 1600    DEFINE PROCEDURE, 'DIAG.7' $
         RECORD "**** BAD UUT ****" $
         'SYS.DIAG-FLAG'(7) = 'SYS.SELECTED' $
         END 'DIAG.7' $
C**********************************************************************
C**********************************************************************
     TEST PROCS $
C**********************************************************************
C**********************************************************************
 1700     DEFINE PROCEDURE, 'TEST.9' $
          'SYS.FLAG' = 'SYS.TRUE' $
          'SYS.ASRT-FLAG' = 'SYS.TRUE' $
```

```
          'AFF-COMP'•TEST' s ] 5
          'OHMMETER.CN*01' s 'A21-2' 5
          '0HMMFTFR.CNX02' 2 'A21-V *
          'PMMMETEP.PffMO?' s 3.2E+05 *
          'OHMMETER#PPW03# s 1.2F+5* S
          'OHMMETER.PRM04' s 250 S
 1705     PERFORM 'OHMMETEP' S
          •PA21•2-»9' s 'OH^MfTFR•PPMO1' $
          'SYS.DEC.01' s 'nHMMfTFR.PES' ^
          COMPARE #PA2t-2*9## GT 3.t9flOOE+05 *
          GOTO STEP 1710 IF GO *
          #SYS,FLA6' s 'SYS,FAISE# S
          #SYS*ASPT-FLAG# s #SYS^FALSE' *
 1710     COMPARE 'SYS^FLAG' #E(5 #5YS*TPUE' *
          GOTO STEP 1715 TF NOGO S
          ©EPFOPM #DTAG*1* %
 1715     #SY^#TEST-FLAG'(1) = $SYS.TESTEO# ^
          END #TFST#q* S
C*********                *****************************************
 1800     DEFINE PPOCE0UPE# #TEST#10# *
          #SYS.FLAS# s #SY^.TRUE# «
          #SYS#ASPT-FLAG' s #SYS,TPUE# S
          #AFF-COMP#TEST# s 2 5
          COMPARE #RA21-2-o*, LT ^#19000E+05 %
          GOTO ?T£P 1805 IF GO *
          fSYS#FLA(?' s #SYS.FALSE* S
          'SYS.A55RT-FLAG' s 'SYS.FALSE' $
 1^05     COMPARE #SYS#FLA«# ,FQ #SYS#TPUE# «
          GOTO STEP 1810 IF WOGO S
          PERFORM #DTAG#4f S
 1810     #SYS.TEST*FLAG#C?) s 'SYS.TESTFD' S
          ENO 'TEST#10# 5
C*********                *****************************************
 1900     DEFINE PROCEDURE, #TFST.11# 3
          #SYS.FLAG# s #SYS.TRUE# *
          'SYS.ASRT-PLAG' s #SYS#TPUE# S
          #AFF-COMP.TEST# s 3 5
          •QHMMETEP^CNXfl1' s #A21-3* S
          'OHMMETFJ9.CMX02' s #A21*i# S
          'OHMMETER.PRM02' = 4 5E+02 S
          'OHMMETER.PRM03' s 7!SF+O;> s
          'OHMMETER.PRM04' s 2800 5
 1905     PE9F0PM #OHMMETE»# S
          #RA21-3*tl# s 'OMMIW!?TER*PPM0!# S
          'SYS.0EC.01* s #OHMMFTFR#RES# $
          #SYS.OEC.02# s U53000E+0? «
          COMPARE *RA21-3*11#UL ^•OinonE+03 > #SYS#DEC*02* LL
             6.01000E+02 - 'SYS.PEC.02' 5
          GOTO STEP 1^10 IF GO S
          #SYS^FLAG# = #SYS.FALSF# S
          #SYS,A<5PT-FLAG' s 'SYS.FALSE' 5
 1910     COMPARE 'SYS.FLAG' ,E0 #SY8.TRUE# «
          GOTO STEP 1915 IF NO^O S
          PERFORM #DIAG#1# $
 1915     #SYS«.TEST-FLAG'(3) s #SYS#TESTED# «
          ENO 'TEST.11* S
             *********************************************************
 2000     DEFINE PROCEDURE, 'TEST.!?' *
          'SYS.FLAG' s '.^YS.TPtlE' 5
          #SYS#ASRT-FLAG' s 'SYS.TRUE' S
```

```
541:             •AFF-COMP.TEST' a 4 «
542:             COMPAPE 'RA21-3-11',  LT a.aAOOOE+O? S
543:             GOTO STEP  2005      TF GO *
,44:             'SYS.FLAG* a 'SYS.FALSE' S
545:             'SYS.ASRT-FLAG' a 'SYS.FALSE' «
546:  2005       COMPARE 'SYS.FLAG'    ,EQ 'SYS.TRUE' 5
547:             GOTO STEP  2010      IF NOGO  «
548:             PERFORM 'DIAG.6' S
549:  2010       'SYS.TEST-FLAG'(a) a 'SYS.TESTFD' 5
550:             END 'TEST.12' S
551: ()*******************************************************
552:  2100       OEFIME PROCEDURE, 'TFST.tV $
553:             'SYS.FLAG' s 'SYS.TRUE' S
554:             'SYS.ASRT-FLAG' a 'SYS.TRUE' S
555:             'AFF-COMP.TEST' a 5 S
556:             COMOAPE 'RA21-3-11',  GT 7.5a000E*O2 s
557:             GOTO STE»  2105      IF GO S
558:             'SYS.FLAG' a 'SYS.FALSE' S
559:             'SYS.ASRT-FLAG' a 'SYS.FALSE' 9
560:  2105       COMPARE 'SYS.FLAG'    ,EQ 'SYS.TRUE' *
561:             GOTO STEP  2110      IF MOGO  S
562:             PERFORM '0TAG.2' $
563:             PERFORM 'DIAG.5' S
564:  2110       'SYS.TEST-FLAG'(5) a 'SYS.TESTED* S
565:             ENO 'TEST. IV S
566: (I*******************************************************
567:  2200       DEFINE PROCEDURE, 'TEST.14' $
568:             'SYS.FLAG' a 'SYS.TRUE' 9
 69:             'SYS.ASRT-FLAG' a 'SYS.TRUE' S
;70:             'AFF-COMP.TEST' a 6 %
571:             '7METER.CNX01' a 'A2J-3' «
572:             '7MF.TER.CNX03' a 'A21-2' 4
573:             'ZMETERI.PRM02' a 0.17E+03 $
574:             'ZMETER'.PRM03' a 0.39E+03 S
575:             'ZMETER.PPMOa' a 1000 S
576:             '7METER.PRMQ5' a 1000 S
577:  2205       PE'FORM 'ZMETEB' «
578:             'ZA21-3-14' a 'ZMETER.PRM01 ' S
579:             'SYS.DEC.01' a 'ZMETFR.RFS' s
 80:             COMPARE 'ZA21-3-14',  U,  1.7?ftftflF+03 aL 3.90000B+02 $
 81:             GOTO STEP  2210      TF GO «
 82:             'SYS.FLAG' a 'SYS.FALSE* S
 83:             'SYS.ASRT-FLAG' a 'SYS.FALSE* 5?
 84:  2210       COMPARF 'SYS.FLAG'    ,E0 'SYS.TRUE' «
 85:             GOTO STEP  2215      TF NOGO  S
 86:             PERFORM 'niAG.l' S
 87:  22t5       'SYS.TEST-FLAG'(6) a 'SYS.TESTED' 5
 88:             END 'TEST.14' 9
 89: (I   ***************************************************^*****
 90:  2300       DEFINE PROCEDURE, 'TEST.15' 9
 91:             'SYS.FLAG' a 'SYS.TRUE' S
 92:             •SYS.ASRT-FLAG' a 'SYS.TRUE' S
 93:             •AFF-COMP.TEST' a 7 S
 94:             COMPARE 'ZA21-3-1*',  GT 3.90000E+rt2 »
 95:             GOTO STEP  2305      IF GO 9
 96:             'SYS.FLAG* a 'SYS.FALSE' $
 97:             'SYS.ASRT-^LAG* a 'SYS.F4LSE' S
 98:  2305       COMPARE 'SYS.FLAG'    ,|?g 'SYS.TRUE' «
 99:             GOTO STEP  2310      IF MOGO  5
 10:             PERFORM '0IAG.2' S
```

```
601:             PERFORM 'DIAG.3' $
602:  2310       'SYS.TEST-FLAG'(7) = 'SYS.TESTED' $
603:             END 'TEST.15' $
604: C*************************************************************
605: C*************************************************************
606: C    SYSTEM VARIABLE INITIALIZATION AND FIRST ENTRY POINT    $
607: C*************************************************************
608: C*************************************************************
609: E  2400      PERFORM 'GET.TIME'  $
610:             RECORD "!X TESTING UUT: A2100-SMALL" $
611:             RECORD  'SYS.CLOCK'(4), "DATE ##/",'SYS.CLOCK'(5), "##
612:                     'SYS.CLOCK'(6), "## TIME", 'PRT.TIME' $
613:             'SYS.TIM' = 'SYS.TIME' $
614:             FOR 'SYS.I' = 1 THRU 'SYS.#DIAGS' THEN $
615:                'SYS.DIAG-FLAG'('SYS.I')= 'SYS.NOT SELECTED' $
616:                'SYS.#TESTS IN CONJ'('SYS.I') = 0 $
617:             END FOR  $
618:             FOR 'SYS.I' = 1 THRU 'SYS.#COMPONENTS' THEN $
619:                'AFF-COMP.STATE'('SYS.I') = 'SYS.DONT KNOW' $
620:                'AFF-COMP.WHERE'('SYS.I') = 0 $
621:             END FOR $
622:             'SYS.#TESTS IN CONJ'(1) = 3 $
 23:             'SYS.#TESTS IN CONJ'(2) = 1 $
 24:             'SYS.#TESTS IN CONJ'(3) = 1 $
 25:             'SYS.#TESTS IN CONJ'(4) = 2 $
 26:             'SYS.#TESTS IN CONJ'(5) = 1 $
 27:             'SYS.#TESTS IN CONJ'(6) = 1 $
 28:             FOR 'SYS.I' = 1 THRU 'SYS.#TESTS' THEN $
 29:                'SYS.TEST-FLAG'('SYS.I') = 'SYS.NOT TESTED' $
 30:             END FOR $
 31: C    BEGINNING OF TESTING        $
 32: C    $
 33: C    CONTROL PRECEDING THE CALL ON THE TEST MODULE 'TEST.9' $
 34:  2500       'SYS.FLAG' = 'SYS.TRUE' $
 35:             PERFORM 'TEST.9' $
 36: C $
 37: C    CONTROL PRECEDING THE CALL ON THE TEST MODULE 'TEST.11' $
 38:  2600       'SYS.FLAG' = 'SYS.TRUE' $
 39:             PERFORM 'TEST.11' $
 40: C $
 41: C    CONTROL PRECEDING THE CALL ON THE TEST MODULE 'TEST.14' $
 42:  2700       'SYS.FLAG' = 'SYS.TRUE' $
 43:             PERFORM 'TEST.14' $
 44: C $
 45: C    CONTROL PRECEDING THE CALL ON THE TEST MODULE 'TEST.10' $
 46:  2800       'SYS.FLAG' = 'SYS.TRUE' $
  7:             PERFORM 'TEST.10' $
  8: C $
  9: C    CONTROL PRECEDING THE CALL ON THE TEST MODULE 'TEST.12' $
  0:  2900       'SYS.FLAG' = 'SYS.TRUE' $
  1:             PERFORM 'TEST.12' $
  2: C $
  3: C    CONTROL PRECEDING THE CALL ON THE TEST MODULE 'TEST.13' $
  4:  3000       'SYS.FLAG' = 'SYS.TRUE' $
  5:             PERFORM 'TEST.13' $
  6: C $
  7: C    CONTROL PRECEDING THE CALL ON THE TEST MODULE 'TEST.15' $
  8:  3100       'SYS.FLAG' = 'SYS.TRUE' $
  9:             PERFORM 'TEST.15' $
  0: C $
```

```
561:  ??00    PgPFOPM 'GET.TIM?' *
562:          3ECORD ••FINISHED TESTING AT% 'PRT.TIMf S
563:          'SYS.TIM' s 'SYS.TIME* - 'SYS.TIM' S
564:          'SYS.CLOCK'(J) s INT f'SYS.TTM'/SfrOni S
565:          #SYS,TIM# s #SYS,TTM# - 3*00*'SYS.CLOCK#(1) $
566:          'SYS.CLOCK'(2) s TNT(#SYS#TIMV^i0) S
567:          'SYS.CLOCK'(3) = #SY$.TIM' • 60*#.SYS.CL0C<'(2) $
568:          PECORO PUPATION " , #PRT#TTME# S
569:          PFMOVF ALL 55
570:          PECQPO "00 YOU WISH TO SEE THE FINAL FAULT ISOLATION 8'
571:             "(Y/N) " S
572:          WAIT-FOP MANMJAL-OATA-60-MOGO S
573:          GOTO STEP 3205 IF MOGO S
574:          PEPFOPM 'PRINT.DONT KWOVt' S
575:          PERFORM 'PRIMT.I?' S
576:          PERFOP^ 'PRINT.IS ^«0T# $
577:          PERFOPM #PPINT#MAY «E# S
578:          PERFORM /PRIMT.MAY «5F (S!OT# $
579:  3205    RECORD "DO YOU WISH TO RERUN THIS PROGRAM? (Y/N)« 8
580:          WAIT-FOR MANIJAL-OATA-GO-WOGO S
581:          GOTO STEP 3210 IP \»0G0 S
582:          RECORO "IP" S
583:          GOTO STEP 2a00 S
584:  3210    RECORD "TERMINATE EQUATE PROGRAM #A3tOO-SMALL' iP" S
585:  3215    FINISH S
586:          TERMINATE EQUATE PROGRAM 'A?1OO-SMALL# S
```

Figure 4.9 ATLAS Program for A2100 Filter Suhcircuit (co

the ohmmeter parameters are assigned values (see lines 482-486). After returning from the procedure, the target variable used in the conjunction is assigned the resistance measured. This variab is used in an assertion to compare its value to 319 Kohm. If the assertion passes, diagnosis 1 is selected.

The program execution start on line 609 (statement number 2400) which is the only entry point to the program. In the prologue, the system variables are initialized and then testing starts on line 634. The sequence of testing is determined by sequence analysis phase of the bottom part of the NOPAL system. Because this sample program does not involve component protection after-diagnoses etc., none of the test procedure calls are preced by checks to determine the run time conditions. If there had been any of these features used in the specification, there would have been additional code between test procedure calls.

After all test are performed, the test duration is printed, and then all ATE devices are removed. If so desired, a synopsis of the fault isolation state is printed. At this point the operator may rerun the same program for another UUT or terminate execution.

The ATLAS program for testing the voltage regulator and time delay circuit is not included in this report. It is availab separately on the accompanying listing and computer tape.

4.6 Evaluation of EQUATE Runs

A. Results from the Filter Subcircuit:

The program discussed in the previous section was used tc test three different A2100 circuit cards. The printouts from EQUATE VII are exhibited in Figure 4.10. The first card teste had a missing capacitor (C2101). Three tests were performed before the failure was detected. The other two cards were goc After card 2 was tested, the fault isolation state was printec as requested. The long repetition in test 1, of cards 2 and 3 is due to the charging time of capacitor C2101. This reflects a deficiency in the test strategy selection and optimization algorithms of the NOPAL system. This is one of the areas wher the current implementation can be improved.

B. Results from the Voltage Regulator and Time Delay Subcircu

Three A2100 cards were tested with the ATLAS program (see Figure 4.11). This program did not have tests which requ probing of the UUT, therefore the ambiguity classes were large The first card tested had a transistor failure which was not c of the failures contained in the failure dictionary. Therefor no diagnosis was selected.

Card 2 contained two physically broken resistors R2105 ar R2109. Because NOPAL generated programs can detect only singl catastrophic failures,multiple failures result in unpredictab selected diagnoses. In this case open failure of R2105 was picked up correctly. However the open of R2105 was not, inste a rather large number of other possible failures were given.

Card·

```
      ...  ...  A2100-SMALL
DATE 12/14/79 TIME 16:41:44
TEST  1:   83571.810 KOHM,   250 MV,   400 KOHM,   1 TIMES, CNX(51,50)
TEST  1: 4580617.473 KOHM,   250 MV,  1000 KOHM,   2 TIMES, CNX(51,50)
TE  T 3:         0.620 KOHM, 2800 MV,     4 KOHM,   2 TIMES, CNX(50,52)
TE  T 6: 110.888 KOHM,-81 DEG, 1004 HZ, 1000 MV,    3.6 KOHM, 80 TIMES, CNX(50,
POSSIBLE FAULTY COMPONENT(S) ---
OPEN(C2101)
FINISHED TESTING AT 16:45:18
DURATION    0: 3:34
DO YOU WISH TO SEE THE FINAL FAULT ISOLATION STATE ? (Y/N)
DO YOU WISH TO RERUN THIS PROGRAM? (Y/N)
```

Card 1

```
 TESTING UUT:  A2100-SMALL
DATE 12/13/79 TIME 18:13:35
TEST  1:  10701.958 KOHM,   250 MV,   400 KOHM,  32 TIMES, CNX(51,50)
TEST  1:  10218.679 KOHM,   250 MV,  1000 KOHM, 119 TIMES, CNX(51,50)
TEST  3:        0.605 KOHM, 2800 MV,     4 KOHM,   2 TIMES, CNX(50,52)
TE  T 6:  0.258 KOHM, -0 DEG, 1004 HZ, 1000 MV,    3.6 KOHM,  2 TIMES, CNX(50,51
** * GOOD UUT ****
FINISHED TESTING AT 18:16:47
DURATION    0: 3:12
DO YOU WISH TO SEE THE FINAL FAULT ISOLATION STATE ? (Y/N)
.IST OF COMPONENTS FOR WHICH NO DIAGNOSIS HAS BEEN MADE:
  1: SHORT(QDR2101)
  2: OPEN(QDR2101)
  3: SHORT(C2101)
  4: OPEN(C2101)
  5: SHORT(R2101)
  6: OPEN(R2101)
 ND OF LIST.
 IST OF COMPONENTS WHICH ARE AFFECTED:
 ** NONE ***
 ND OF LIST.
 IST OF COMPONENTS WHICH ARE NOT AFFECTED :
 ** NONE ***
 ND OF LIST.
 IST OF COMPONENTS WHICH MAY BE AFFECTED:
  1: NOMINAL(ALL-COMPS)
 ND OF LIST.
 IST OF COMPONENTS WHICH MAY NOT BE AFFECTED :
 * NONE ***
 D OF LIST.
  YOU WISH TO RERUN THIS PROGRAM? (Y/N)
```

Card #3

```
 TESTING UUT:  A2100-SMALL
TE 12/13/79 TIME 18:17:51
ST  1:  10270.127 KOHM,   250 MV,   400 KOHM,  51 TIMES, CNX(51,50)
ST  1:  10065.801 KOHM,   250 MV,  1000 KOHM, 134 TIMES, CNX(51,50)
ST  3:        0.562 KOHM, 2800 MV,     4 KOHM,   2 TIMES, CNX(50,52)
 T  6:  0.261 KOHM, -0 DEG, 1003 HZ, 1000 MV,    3.6 KOHM,  2 TIMES, CNX(50,51)
 * GOOD UUT ****
NISHED TESTING AT 18:21:14
RATION    0: 3:23
 YOU WISH TO SEE THE FINAL FAULT ISOLATION STATE ? (Y/N)
 YOU WISH TO RERUN THIS PROGRAM? (Y/N)
RMINATE EQUATE PROGRAM 'A2100-SMALL'
```

.gure 4.10 EQUATE Printouts for the Filter C...

TESTING OUT: AS2.OO Card #

```
DATE 12/14/7? TIME 13:40:34
TEST  1:        1.537 KOHM,   230 MV.      4 KOHM*   2 TIMES* CNX(39* 41)
TEST  3:        0.301 KOHM*   250 MV,      4 KOHM*   3 TIMES* CNX(61* 39)
TEST  5:       27.662 KOHM*   230 MV,     40 KOHM*  16 TIMES* CNX(63*61)
TF^T  8:       49.643 KOHM*   250 MV,    400 KOHM*  10 TIMES, CNX <23* 63)
TL ; 11:        1.471 KOHM*  2300 MV,      4 KOHM*   2 TIMES* CNX (39, d3)
TEST 14:        1.127 KOHM*  2800 MV*      4 KOHM,   2 TIMES, CNX(25*63)
TEST 17:        1. 166 KOHM* 2300 MV*      4 KOHM.   4 TIMES, CNX(63* 41)
TEST 20:   0. 000 KOHM*  2 DEG*  1004 HZ*  1000 MV,    3.6 KOHM*  33 TIMES*  CNX (41* 63
TEST 22:   0. 633 KOHM* -3 DEG,  1003 H2*  1000 MV*    3.6 KOHM*   2 TIMES*  CNX (41* 23
   ATTENTION OPERATOR:  UUT IS SEIKO POWERED NOW
TEST 24: APPLIED DC2A* 25. 300 V. CNX HI 39 LO 41 .
         MEASURED 0. 0133 AMPS THRU DC2A.
TEST 24: MEASURED 23. 497 V, CNX HI 61 LO41 .
   ATTENTION OPERATOR:  UUT IS BEING POWERED NOW
TEST 26: APPLIED 0C2A, 23. 300 V* CHX HI 39 LO 41 .
         MEASURED 0. 0123 AMPS THRU DC2A.
TEST 26: MEASURED 3. 170 V* CNX HI 63 LO 41 .
FINISHED TESTING AT 13: 47i 5
DURATION   0:  6:31
DO YOU WISH TO SEE THE FINAL FAULT ISOLATION STATE ? (Y/N)
DO YOU WISH TO RERUN THIS PROGRAM? (Y/N)
```

TESTIIMG UUT: AS1OO Card # 2

```
DATE 12/14/79 TIME 18:34: 4
TEST  1:        1. SOO KOHM*   230 MV,      4 KOHM*   2 TIMES. CNX (59, 41)
TEST  3:        0. 483 KOHM*   230 MV,      4 KOHM/   2 TIMES*  CNX(61*39)
TEST  5:      34. 991 KOHM*   230- MV,    40 KOHM*  10 TIMES*  CNX (63* 61)
TF^T 3;  74830. 566 KGHM*   250 MV*   400 KOHM,    1 TIMES,  CNX (25* 63)
TL.f 11:       1.302 KOHM*  2S00 MV*      4 KOHM*   2 TIMES,  CNX(59,63)
TEST 14:     666. 203 KOHM,  2S00 MV,      4 KOHM*  13 TIMES,  CNX(23* 63)
TEST 17:       7. 450 KOHM*  2300 MV*      4 KOHM*   6 TIMES*  CNX(63,41)
TEST 17:      10. 752 KOHM*  2800 MV,     40 KOHM*  10 TIMES, CNX < 63* 41)
TEST 20:  0. 000 KOHM* 93 DEG*  1004 H2*  1000 MV*    3.6 KOHM,  39 TIMES*  CNX (41*6^
TEST 22:  4. 278 KOHM* -83 DEG* 1004 HZ*  1000 MV*    3.6 KOHM,   6 TIMES,  CNX(41*2!
POSSIBLE FAULTY COMPONENTS)_____
C0LL-0PSN<QQ2i01) OR BASE-OPEN(QQ2101) OR C0LL-0PEN<QQ2102) OR BASE-OPEN(QQ210:
POSSIBLE FAULTY COMPONENTS)_____
OPEN<QDR2102)
POSSIBLE FAULTY COMPONENTS)_____
OPEN<QDR2106)
POSSIBLE FAULTY COMPONENTS)_____
OPEN<R2103) OR OPEN(R2107)
POSSIBLE FAULTY COMPONENTS)_____
0PEN(C2104)     •
POSSIBLE FAULTY COMPONENT(S) ____
OPEN<R2109)
   ATTENTION OPERATOR:  UUT IS BEING POWERED NOW
TEST 24: APPLIED DC2A* 23. SOO V* CNX HI 39 LO 41 .
         MEASURED 0. 0109 AMPS THRU 0C2A.
TEST 24: .MEASURED 23. 499 V, CNX HI 61 LO 41 .
   ATTENTION OPERATOR:  UUT IS BEING POWERED NOW
TEST 26: -APPLIED DC2A, 23. 300 V* CNX HI 59 LO 41 .
         MEASURED 0. 0107 AMPS THRU DC2A.
Tr  * 26: MEASURED 7. S49 V* CHX HI 63 LO 41 .
FINISHED TESTING AT 19:  1:33
DURATION   0:  7: 29
DO YOU WISH TO SEE THE FINAL FAULT ISOLATION STATE ? (Y/N)
DO YOU WISH TO RERUH THIS PROGRAM? <Y/N)
```

gure 4,11 EQUATE Printouts for the Voltage Regulator and Time Delay

```
 TESTING UUT: A2100                                                    Card #
DATE 12/14/79 TIME 19: 4:42
TEST  1:        1.631 KOHM,  250 MV,     4 KOHM,   2 TIMES, CNX(59,41)
TEST  3:        0.533 KOHM,  250 MV,     4 KOHM,   2 TIMES, CNX(61,59)
TEST  5:       34.336 KOHM,  250 MV,    40 KOHM,   8 TIMES, CNX(63,61)
TE^T  8:       51.169 KOHM,  250 MV,   400 KOHM,  11 TIMES, CNX(25,63)
TL ; 11:        1.450 KOHM, 2800 MV,     4 KOHM,   2 TIMES, CNX(59,63)
TEST 14:        1.119 KOHM, 2800 MV,     4 KOHM,   2 TIMES, CNX(25,63)
TEST 17:        1.009 KOHM, 2800 MV,     4 KOHM,   4 TIMES, CNX(63,41)
TEST 20:  0.000 KOHM,  3 DEG, 1004 HZ, 1000 MV,   3.6 KOHM,  105 TIMES, CNX(41,6
TEST 22:  0.716 KOHM, -9 DEG, 1004 HZ, 1000 MV,   3.6 KOHM,   3 TIMES, CNX(41,25
   ATTENTION OPERATOR:  UUT IS BEING POWERED NOW
TEST 24: APPLIED DC2A, 25.500 V, CNX HI 59 LO 41 .
         MEASURED 0.0173 AMPS THRU DC2A.
TEST 24: MEASURED 21.068 V, CNX HI 61 LO 41 .
   ATTENTION OPERATOR:  UUT IS BEING POWERED NOW
TEST 26: APPLIED DC2A, 25.500 V, CNX HI 59 LO 41 .
         MEASURED 0.0169 AMPS THRU DC2A.
TEST 26: MEASURED 12.697 V, CNX HI 63 LO 41 .
FOLLOWING FAILURES (INCLUDING NOMINAL CASE)
 WERE NOT DIAGNOSABLE ---
NOMINAL(ALL-COMPS) OR OPEN(QDR2103) OR
 OR SHORT(QDR2104) OR OPEN(QDR2105) OR SHORT(QDR2105) OR R
 COLL-OPEN(QQ2103) OR BASE-OPEN(QQ2103) OR EMIT-OPEN(QQ2103)..
FINISHED TESTING AT 19:12:13
DURATION    0: 7:31
DO YOU WISH TO SEE THE FINAL FAULT ISOLATION STATE ? (Y/N)
DO YOU WISH TO RERUN THIS PROGRAM? (Y/N)
TERMINATE EQUATE PROGRAM 'A2100'
```

Figure 4.11 EQUATE Printouts for the Voltage Regulator and Time Delay Subcircuits (continued)

Card 3 was a good card. Because the test design in this particular program did not utilize probing (to speed testing), the nominal equivalence class contained a large number of semi-conductor failures. In a test design which uses probing, these possibilities were removed. The program included which is the accompanying tape has the fault isolation capability shown in Table 4.7. In this program all transistor failures are diagnosable.

CHAPTER V

GENERATION OF A TEST PROGRAM AUDIO AMPLIFIER CARD - A5100

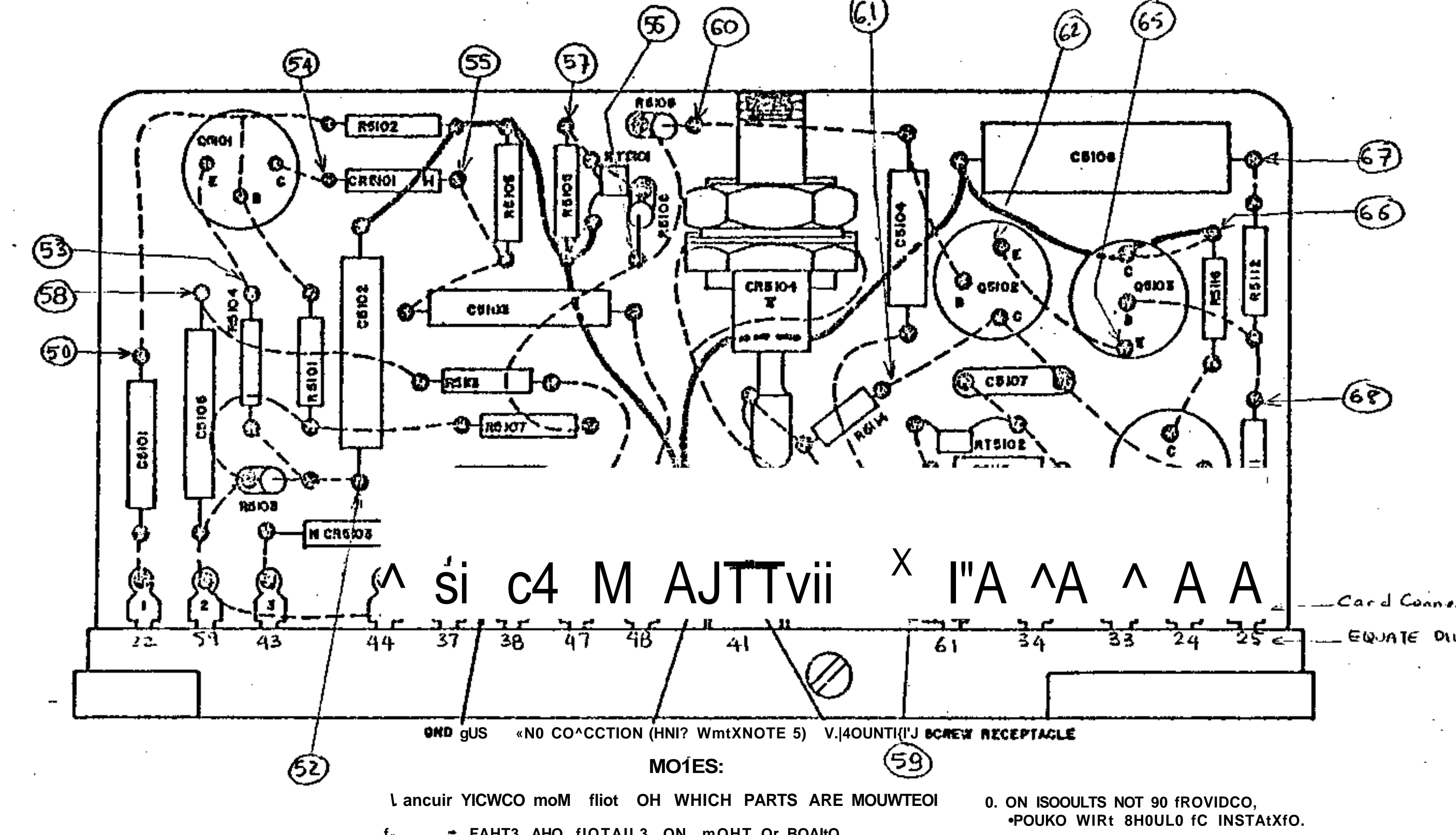
The generation of a test program to diagnose and isolate single catastrophic failures in the A5100 audio amplifier circ card of the AN/VRC-12 radio is described in the following six sections. Section 1 presents the theory of operation for the circuit. This description follows the theory given is TM5820-409-35-34 Section A, pages 19-21. Section 2 contains the input supplied to the top part of the NOPAL system. Each input option is briefly explained. An overview of the tables generated by the system is given Section 3. The NOPAL specifi cation of the tests based on these tables is explained in Section 4. The flowchart of the EQUATE ATLAS program which is generated from the NOPAL specification is described in Section Finally in Section 6, the printouts obtained by running this program on either EQUATE V or VII are exhibited an evaluated.

5.1 AUDIO AMPLIFIER ASSEMBLY-A5100: THEORY OF OPERATION

The module provides two outputs, a high-level audio amplifier output and a low-level monitor amplifier output (Figure 5.1). The amplifiers are expected in the 300 through 3000 KHertz audio range. The monitor amplifier is described under paragraph A, and the audio amplifier is described under paragraph B.

A. A Simplified schematic diagram of the monitor amplifier is shown in Figure 5.2. The monitor amplifier provides a fixed level audio output which is independent of the setting of the volume control. Capacitor C5101 couples the audio signal at the output of filter FL5001 to the base of Q5101. The amplifie output across load resistor R5105 is coupled through capacitor C5103 to the interphone amplifer AM-1780/VRC. During reception of transmitted signals (no squelch), Q5101 is powered from the 16-Volt power supply. During squelch operation, the power supp is disconnected from the monitor amplifer, thereby disabling th stage; diode CR5101 prevents the transfer of an audio signal through the base-to-emitter circuit of Q5101. Resistor R5104 provides emitter degeneration for gain stability. Voltage divi resistor R5101 and R5102 develop the fixed bias portion of the emitter-to-base bias. Resistors R5103 and R5104 establish the self-bias portion of the emitter-to-base bias and are used for current stabilization. Capacitor C5102 is an audio bypass capacitor.

B. A simplified schematic diagram of the audio amplifier is shown in Figure 5.3. The audio amplifier stages amplify freque from 300 to 3000 hertz. The final amplifier stage uses power



MO1ES:

\ ancuir YICWCO moM fliot OH WHICH PARTS ARE MOUWTEOI

f# . . . FAHT3 AHO fIQTAIL3 ON mOHT Or BOAltO.

1. - - - WIRIMfl ON BACK OF DOAAO.

4 m....• wtfIIM« OH FRONT OF BOARD.

0. ON ISOOULTS NOT 90 fROVIDCO, •POUKO WIRt 8H0UL0 fC INSTAtXfO.

figure 5.1 Assembly A5100, Parts Location and Wiring Diagram.

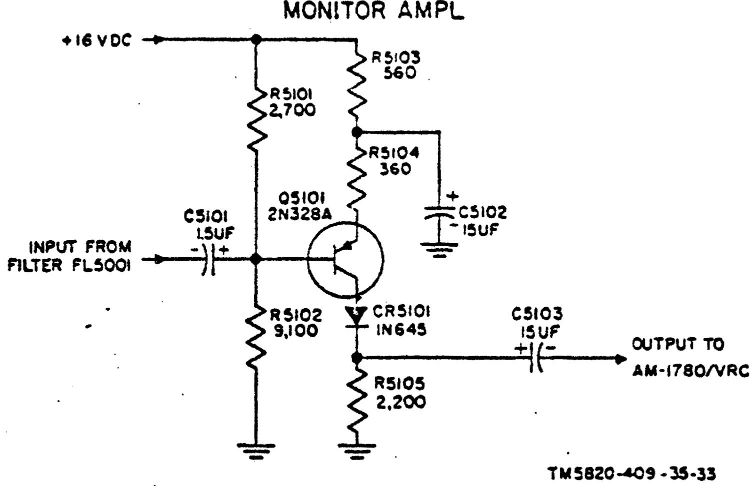


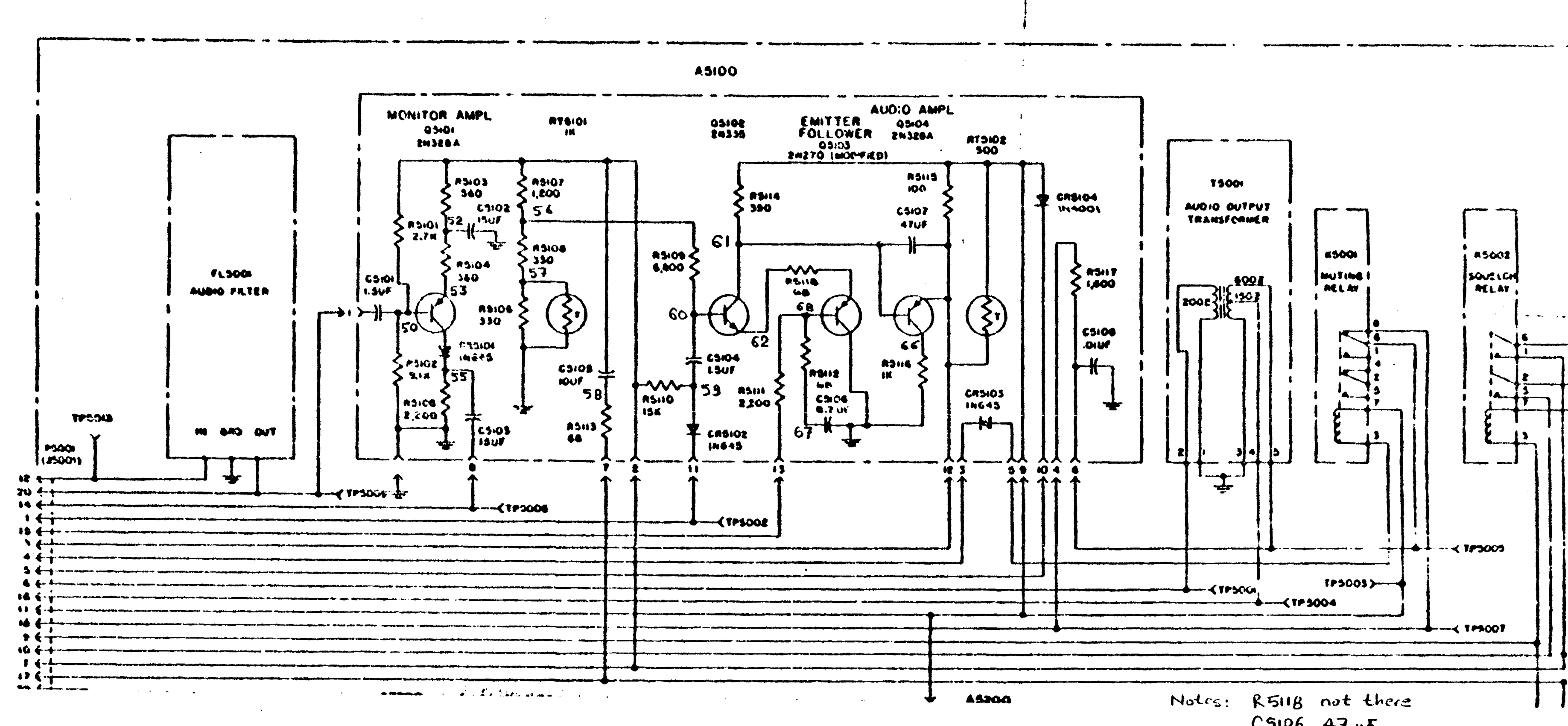
Figure 5 . 2 *Monitor amplifier, simplified schematic diagram.*

R5113
68
C5105
10UF
+16 VDC
R5106
330
+16 VDC
TCHED BY
CH RELAY
K5002
R5107
1,200
R5108
330
R5110
15K
R5109
6,800
RT5101
1K
INPUT
FROM
FILTER
FL5001
VOLUME
R101
CR5102
1N645
C5104
1.5UF
AUDIO AMPL
-25.5 VDC
R5114
330
R5115
100
RT5102
500
C5108
.01UF
R5117
1,600
MUTED
OUTPUT
MUTING
SIGNAL
TO GRD
WHEN
XMTG
CR5104
1N3565
CR5103
1N645
K5001
C5107
.47UF
Q201
(Q402)
2N297A
Q5104
2N328A
T5001
R202
(R402)
22
UNMUTED
OUTPUT
Q5102
2N335
R5116
1K
R5111
2,200
EMITTER
FOLLOWER
Q5103
2N270
R5112
91
C5106
47UF

NOTE:
REFERENCE DESIGNATIONS IN PARENTHESES ( ) REFER TO RT-246/VRC AND RT-524/VRC.

TM5820-409-35-34

Figure 5 . 3 *Audio amplifiers, simplified schematic diagram.*


A5100
MONITOR AMPL
Q5101
2N328A
RT5101
1K
Q5102
2N338
EMITTER
FOLLOWER
Q5103
2N270 (MODIFIED)
AUDIO AMPL
Q5104
2N328A
RT5102
500
T5001
AUDIO OUTPUT
TRANSFORMER
K5001
MUTING
RELAY
K5002
SQUELCH
RELAY
FL5001
AUDIO FILTER
IN GRD OUT
TP5002
TP5003
TP5004
TP5005
TP5006
TP5007
TP5008
A5200
Notes: R5118 not there
C5106 47 µF

transistor Q201 (Q402) and resistor R202 (R402) which are not on the amplifier module. They are mounted in a heatsink on the case. The output of the audio and squelch preamplifier feeds through low-pass filter FL5001, to volume control R101, diode CR5102, and capacitor C5104 to the base of Q5002. The amplified output across load resistor R5114 is direct-coupled to the base of Q5104, amplified and direct-coupled to the base of Q201. The amplified output across voltage divider, R5111, R5112 and C5106, in parallel with resistor R202 and the primary winding of transformer T5001. A part of the output is coupled back to the collector of Q5103, across degenerative ac feedback network of R5111, R5112, and C5102. The circuit raises input impedance, reduces audio distortion, and stablizes amplifier gain. The other output across R202 and the primary winding of T5001 is coupled to the secondary of T5001. The output across the full secondary winding of T5001 is coupled through the contacts of relay R5001 to drive the loudspeaker. The output across the center tap of the secondary winding provides an unmuted output to the headphones. In transmit mode, a ground is supplied to one side of muting relay K5001, causing it to energi This removes the short across resistor R5117, inserting a 1600 o resistance in series with the loudspeaker, resulting in muted audio output. Capacitor C5108 is an arc suppressor for relay K5

During reception of transmitted signals (no squelch), 16 volts dc is connected to voltage divider R5107, R5108, R5106, and RT5101. The voltage present at the junction of R5107 and R5 is applied through isolating resistor R5109 to the base of Q5102

and establishes the fixed-bias portion of the emitter-to-base bias. The effective resistance of Q5103, which increases or decreases with variations in temperature, provides bias to the emitter of Q5102. The collector voltage of Q5102 establishes base voltage for Q5104. Temperature-compensated voltage divid R5115 and RT5102 establishes the voltage supplied to the emitt of Q5104. Resistor R5106 develops the collector-to-base bias for Q5104. The emitter voltage of Q5104 establishes the base voltage of Q201(Q402). Diode CR5104 provides a constant volta drop of 0.8 volt dc to the emitter of Q201 (Q402), keeping its emitter voltage constant. This allows a reverse bias to be applied to the base-to-emitter function to prevent thermal runaway at high temperatures. The voltage drop across power resistor R202 (R402) and the primary winding of transformer 75001 establishes the collector voltage for Q201 (Q402). Dc feedback is used to maintain constant collector currents for t transistors to prevent thermal runaway. For the base of trans Q201 (Q402) the network, consisting of resistors R5115 and R51 thermistor RT5102, and Q5104, appears as a voltage divider in which Q5104 is a variable resistor whose value is controlled by its emitter-to-base bias. For the emitter of Q5102, transi Q5103 appears as a variable resistance to ground whose value is controlled by its emitter-to-base bias. An increase in temperature lowers the resistance of a thermistor. An increas in temperature is usually due to an increase in collector currents. The biasing circuits are designed such that a decre in the thermistor resistance results in driving the transistor toward cutoff and returns the collector current to its origina value.

Capacitor C5105 and resistor R5113 produce a time delay across terminals 2 and 7 of squelch relay K5002 to prevent key clicks from occuring at the audio output during squelch operation as the 16 volt dc line is disconnected.

5.2 NOPAL Input

The input given to the NOPAL system to generate a test program for the monitor and audio amplifiers is shown in Figure 5.5. A few of the isolated components on the card (CR5103, CR5104, R5117 and C5108) are not included in the circ description because they are not a part of the amplifier circu A test program to test them is generated separately.

The resistors and capacitors are described completely in the circuit description. The diode and transistor models are included from the model library 2. The models are shown in Appendix 1. During testing it was observed that resistor R511 does not exist physically on any of the circuit cards that wer available. Also capacitor C5106 has been charged to 47μF from 8.2μF. The circuit description was accordingly charged to incorporate the capacitor change. R5118 was retained as is because of its low resistance in a low current base circuit.

The interface device provided by RCA to test the AN/VRC-1 cards had an additional resistor (RUUT1) 33 Kohm which was not shown on the circuit schematic diagram. This is a capacitor discharge resistor grounding circuit node 1. RUUT3 was measur to be 482 ohms. In the documentation it was shown to be 560 c The measured quantities with +-10% tolerances are used in the circuit description. All of the remaining resistors and capac are assigned 10% tolerance. The diode parameters have 5%, and transistor parameters have 0.5% tolerance.

The test requirements given under the circuit descriptior are the same as the requirements described for the A2100 card.

```
CIRCUIT J>ES CRIPTIOV ' ' A51E0 * DEFAULT ' AUDIO AMPLIFIER - ' ' *
•CIRCUIT
: THIS IS MONITOR AMPLIFIER
C5101 1      50    1.5UF              : FAILS
R5102      50    3     9.1K            : FAILS
R51Q1      50    2     2.7X            : FAILS
R51C3       2   52     560            : FAILS
R5104      52   53'    360            : FAILS
C5102      52    0     15UF            : FAILS
QQ5>101     5* * 1   53 * 2    5 3 = 3          : FAILS
*LiB2      TR 2N329A
Q*
QDR51C1    54 * 1   55 * 3          : FAILS
*LIB2      01N645
Q*
R5105      55    3     2.2K           : FAILS
C5103      55    S     15UF           : FAILS
: THIS IS AUDIO ATFLIFIER
R5107       2    56    1.2K     : FAILS
R5108      56    57    332    : FAILS
R51C6      57     0    330    : FAILS
RT5101     57    0-     1K       : FAILS
C5105       2    5c     10UF    : FAILS
R5113      5s     7     68    : FAILS
R5110       2    59    15K   :   FAILS
:
                         COUPLING BETWEEN MONITOR AMPLIFIER
,
                              AND EMITTER FOLLOWER
R5109      55    60    6S3C  :  FAILS
*
                          COUPLING BETWEEN "OtflTOR AMPLIFIER
:
                              AND EMITTER FOLLOWER
805102     $1 * 1    60 * 2    62 * 3         : FAILS
•LIB2      TR2N33S
Q*
R5114      61       9      33C         :I  FAILS
R5115       9      12      103         :I  FAILS
C51.07     61      12      C.47UF          :  FAILS
C51C4      59      6?      1 .5UF         :  FAILS
Q0R5132    59 * 1    11 = 3          :  FAILS
*LI32      D1N645
Q*
R5118      62      (!S      6£          :   FAILS
QQ5103      0 * 1      6E * 2    65 * 3          :   FAILS
*LI52      TR2N404A

R5111      68      13      2200          :   FAILS
R5112      68      67      6S          :   FAILS
C51C6      67       0      47UF          :   FAILS
R5116      66       0      IK          :   FAILS
QQ5134     66 s 1     61 = 2    12 = 3          :   FAILS
*LI52      TR2N329A
Q*
RT51O2      9   12      500      : FAILS
: THE FOLLWING ARE UUT INTERFACE RESISTANCES
RUUT1    1     0      33K
```

Figure 5.5 NOPAL Input For A5100

```
RUUT2   8     0      153
RUUT3   11    0      482
*MODIFY  1  0.10  0.10    >
    R5101 R5102 R5103 R5104 C5101 C5102   >
    R5105 C5103 R5107 R5108 R5106 RT5101  >
    C5105 R5113 R5110 R5109 R5114 R5115  >
    C5107 C5104 R5118 R5111 R5112 C5106  >
    R5116 RT5102 RUUT1 RUUT2 RUUT3
*MODIFY  2   0.05    0.05    >
        QDR5101.ID QDR5101.CT QDR5101.CD       >
        QDR5102.ID QDR5102.CT QDR5102.CD
*MODIFY 3  0.005  0.005           >
 QQ5101.IN QQ5101.II QQ5101.CED QQ5101.CET QQ5101.CCD QQ5101.CCT  >
 QQ5102.IN QQ5102.II QQ5102.CED QQ5102.CET QQ5102.CCD QQ5102.CCT  >
 QQ5103.IN QQ5103.II QQ5103.CED QQ5103.CET QQ5103.CCD QQ5103.CCT  >
 QQ5104.IN QQ5104.II QQ5104.CED QQ5104.CET QQ5104.CCD QQ5104.CCT
TEST_TERMINALS     J8     PC BOARD EDGE CONNECTOR
0      GND
1      A51_1
2      A51_2
7      A51_7
8      A51_8
9      A51_9
11     A51_11
12     A51_12
13     A51_13
ACTEST_TERMINALS     J8      PC  BOARD EDGE CONNECTOR
0      GND
1      A51_1
2      A51_2
7      A51_7
8      A51_8
9      A51_9
11     A51_11
12     A51_12
13     A51_13
OBJECTIVES    STANDARD
 100.0%   DIAGNOSIS
  50.  2   AMBIGUOUS
  60.  4   AMBIGUOUS
ACCURACY MINIMAL
    0.50E-02                        ZERO DESCRIMINATION
    0.10E+02                        INACCURACY IN %
  3                SIGNIFICANT DIGITS
  1               SORT WITHIN TEST ONLY
  1               OPTIMIZE LOGIC
  1               MISSING FAILURES SAME AS NOMINAL
    5.00E+00    10.00E+05         RESISTANCE
    1.50E+01    10.00E+03         IMPEDANCE
    0.10E-03    00.50E+00         CURRENT
    0.10E+00    03.00E+01         VOLTAGE
   1   1
ACBIAS    DC OPERATING POINT IS DECIDED BY THE FOLLWING DC SUPPLY
BEGIN    UUT IS BEING POWERED NOW

RSUP1   9  0    0.1    E   25.5V
RSUP2   2  0    0.1    E    16V
RSUP4   13 0    0.1    E    0.0 V
INITIAL_CONDITIONS    POWERUP
BEGIN     UUT IS BEING POWERED NOW
RSUP1   9  0    0.1    E    25.5V
RSUP2   2  0    0.1    E    16V
RSUP4   13 0    0.1    E    6.0V
END
END-INITIAL
```

Figure 5.5 NOPAL Input For A5100 (contin

There are two initial conditions specified. The first one sets power supply RSUP4 to 0.0 volt, thereby turning the audio amplifi off. The second initial condition changes the power supply volta level to 6.0 volts which turns on all the transistors. These levels force the amplifier to operate at its limits.

5.3 Evaluation of Tables Generates

The failure dictionary for the A5100 card has initially 81 failure modes. 19 failures are due to resistors which are remove from consideration after circuit simulation. If it becomes desirable to do so, a test program searching for resistor shorts can be readily generated since all necessary failure symptoms are available in the simulation results.

The binary valued diagnosis matrix and assertions table has 162 rows which are generated from 76 different test setups. These tables are not included in this report. They are available on the listings and computer tape accompanying this report.

The ambiguity analysis indicates that with these tests 95% fault diagnosis is possible (see Table 5.1). 30 out of 62 failur can be uniquely isolated. The open failures of the two thermisto RT5101 and RT5102 could not be distinguished from the nominal circuit behavior. This is not surprising because these thermisto are in parallel with low valued resistors and the tolerances on these components effectively hide their open failure. In fact as it was described in the theory of operation of A5100 circuitry it was explained that these thermistors function when the operati temperature of the card increases. This condition arises when the card has been operating at high output levels for some time. Since such a long operation time could not be allowed on an ATE,

EQUIVALENCE CLASS	K-AMBIGUITY	FAULT ISOLATION PERCENTAGE		FAILURE MODES INCLUDED
		CLASS	CUMULATIVE	
NOMINAL	1	1.6%		ALL COMPONENTS NOMINAL
O-DIAGNOSIS	3	4.8%		NOMINAL(ALL_COMPS), OPEN(RT5101), OPEN(RT5102).
2	2	3.2%	3.2%	OPEN(C5101), OPEN(R5101).
3	1	1.6%	4.8%	SHORT(C5101).
4	4	6.5%	11.3%	OPEN(R5102), COLL_OPEN(QQ5101), BASE_OPEN(QQ5101), EMIT_OPEN(QQ5101).
5	1	1.6%	12.9%	OPEN(R5103).
6	1	1.6%	14.5%	OPEN(R5104).
7	1	1.6%	16.1%	OPEN(C5102).
8	1	1.6%	17.7%	SHORT(C5102).
9	3	4.8%	22.6%	BC_SHORT(QQ5101), EC_SHORT(QQ5101), SHORT(QDR5101).
10	1	1.6%	24.2%	BE_SHORT(QQ5101).
11	1	1.6%	25.8%	OPEN(QDR5101).

Table 5.1 A5100 Ambiguity Report

EQUIVALENCE CLASS	K-AMBIGUITY	FAULT ISOLATION PERCENTAGE		FAILURE MODES INCLUDED
		CLASS	CUMULATIVE	
12	1	1.6%	27.4%	OPEN(R5105).
13	1	1.6%	29.0%	OPEN(C5103).
14	1	1.6%	30.6%	SHORT(C5103).
15	1	1.6%	32.3%	OPEN(R5107).
16	1	1.6%	33.9%	OPEN(R5108).
17	1	1.6%	35.5%	OPEN(R5106).
18	2	3.2%	38.7%	OPEN(C5105), OPEN(R5113).
19	1	1.6%	40.3%	SHORT(C5105).
20	1	1.6%	41.9%	OPEN(R5110).
21	1	1.6%	43.5%	OPEN(R5109).

AMBIGUITY REPORT (PAGE 3)

EQUIVALENCE CLASS	K-AMBIGUITY	FAULT ISOLATION PERCENTAGE		FAILURE MODES INCLUDED
		CLASS	CUMULATIVE	
22	1	1.6%	45.2%	COLL_OPEN(QQ5102).
23	5	8.1%	53.2%	BASE_OPEN(QQ5102), EMIT_OPEN(QQ5102), OPEN(R5118), BASE_OPEN(QQ5103), EMIT_OPEN(QQ5103).
24	1	1.6%	54.8%	BC_SHORT(QQ5102).
25	1	1.6%	56.5%	BE_SHORT(QQ5102).
26	3	4.8%	61.3%	EC_SHORT(QQ5102), BC_SHORT(QQ5104), EC_SHORT(QQ5104)
27	1	1.6%	62.9%	OPEN(R5114).
28	1	1.6%	64.5%	OPEN(R5115).
29	1	1.6%	66.1%	OPEN(C5107).
30	2	3.2%	69.4%	SHORT(C5107), BE_SHORT(QQ5104).
31	1	1.6%	71.0%	OPEN(C5104).

QUIVALENCE CLASS	K-AMBIGUITY	FAULT ISOLATION PERCENTAGE		FAILURE MODES INCLUDED
		CLASS	CUMULATIVE	
32	1	1.6%	72.6%	SHORT(C5104).
33	1	1.6%	74.2%	OPEN(QDR5102).
34	1	1.6%	75.8%	SHORT(QDR5102).
35	2	3.2%	79.0%	COLL_OPEN(QQ5103), EMIT_OPEN(QQ5104).
36	2	3.2%	82.3%	BC_SHORT(QQ5103), SHORT(C5106).
37	1	1.6%	83.9%	BE_SHORT(QQ5103).
38	1	1.6%	85.5%	EC_SHORT(QQ5103).
39	1	1.6%	87.1%	OPEN(R5111).
40	2	3.2%	90.3%	OPEN(R5112), OPEN(C5106).
41	1	1.6%	91.9%	OPEN(R5116).

EQUIVALENCE CLASS	K-AMOIöUITt	MULT ISOLATION PERCENTAGE		FAILURE NODES INCLUDED
		CLASS	CUMULATIVE	
42	2	3.2*	95.2X	COLL J>PEN<QQ510O9 BASE.OPEN(QQ51O4).

Table 5.1 A51OO Ambiguity Report (continued)

FAULT ISOLATION SUMMARY

DESIRED AND ACHIEVED LEVEL OF CUMULATIVE
FAULT ISOLATION PERCENTAGE

K-AMBIGUITY	DESIRED C.F.I.P.	ACHIEVED C.F.I.P.	CLASS F.I.P.	NUMBER
1	0.0%	48.4%	48.4%	30
2	50.0%	71.0%	22.6%	7
3	50.0%	80.6%	9.7%	2
4	80.0%	87.1%	6.5%	1
5	80.0%	95.2%	8.1%	1

NUMBER OF FAILURE MODES : 62
NUMBER OF EQUIV. CLASSES : 42
DESIRED LEVEL OF DIAGNOSIS: 100.0%
ACHIEVED LEVEL OF DIAGNOSIS: 95.2%
FAULT ISOLATION IS NOT SATISFACTORY.

Table 5.1 A5100 Ambiguity Report (continu

an alternate way would have been to manually warm the termist
to observe a decrease in the termistor resistance or output l
It was decided that doing such a test at this initial investi
stage was unnecessary.

The largest ambiguity group (equivalence class 23) has 5
possible failures. One of the failures is due to resistor R5
which has been omitted during manufacturing of the A5100 card
The remainder of the failures are due to transistors Q-5102
Q5103. The next largest ambiguity group (class 4) is due to
the failures of resistor R5102 and transistor Q5101.

It should be observed that all of the failure functions
an equivalence class tend to be the same (i.e. all open or al
short). If the failures are due to open, the affected compon
are generally in series and no probing is done (it is physica
impossible) at their common node. If the failures are due to
short, the affected components are generally in parallel and
would require the physical removal of a component to determin
which one is at fault. Due to the design of the circuit abou
10 probe tests had to be included to achieve this ambiguity l

Table 5.2 is a summary of the test setup optimization
phase. Out of 76 candidate tests only 28 were found to be su
while enabling a top down fault isolation design. The first
test selected is a dc-power up test which immediately splits
large number of possible failures from the nominal. Then, te
are selected as the number of possibilities in each as class
reduced.

INDIVIDUAL ANO *iCIKi* LNT*OPY VALUCS

SEQ	STIM	MEAS	ASSF	EfcTftOPY	JOINT EfcTROPY	EQU1V. CLASS
75	63	10	15?	C.8Z6	0.826	2
55	52	5	114	0.605	1 .360	3
70	58	1	144	Q.6t3	1 .851	6
56	52	6	116	0.449	2.256	9
76	64	10	161	0.503	2.643	13
37	37	1	t7	0.394	2.956	16
68	56	1	138	0.394	3.262	20
40	40	1	75	0.3*4	3.528	23
72	60	1	n:	0.3*4	3.746	26
38	38	1	7C	C.263	3.053	29
41	41	1	7f	0.2t3	4.146	31
32	32	1	5?	0.263	4.312	33
*»7	47	1	95	0.263	4.466	35
69	57	1	141	0.3*4	4.6 08	37
50	50	1	1C4	0.229	4.746	38
49	49	1	1C1	0.192	4,859	40
8	8	1	14	0.2*9	4.961	42
74	62	1	156	0.2t3	5.057	44
57	52	7	119	0.333	5.141	46
1	1	1	1	CC96	5.199	47
3	3	1	6	Q.0V6	5.255	48
65	53	1	131	0.CV6	5.309	49
73	61	1	152	0.192	5.360	50
2	2	1	3	0.333	5.408	51
54	52	4	112	0.573	5.453	52
5	5	1	9	0.2b4	5.493	S3
39	39	1	73	0.0V6	5.517	54
67	55	1	135	0.263	5.542	55
4	4	1	9	O.OCO	5*542	55
6	6	1	11	O.OCO	5.542	55
7	7	1	12	C234	5.542	55
9	9	1	16	0.096	5.542	55
10	10	1	18	C096	5.542	55
11	11	1	20	0.096	5.542	55
12	12	4	ZZ	0.2fc4	5.542	55
13	13	1	£4	0.0V6	5.542	55
14	14	1	*lt*	C.2&4	5.542	55
15	15	1	28	O.OCO	5.542	55
16	16	1	29	0.096	5.542	55
17	17	1	31	0.333	5.542	55
18	18	1	34	C2&4	5.542	55
19	19	1	36	0.167	5.542	55
20	20	1	38	0.2*4	5.5*2	55
i 1	21	1	40	0.229	5.542	55
22	22	1	42	C.CV6	5.542	55
23	23	1	44	O.CüO	5.542	55
24	24	1	45	0.0*6	5.542	55
*5	25	1	47	CCCO	5.542	55
26	26	1	48	COoO	5.542	55
27	27	1	49	0.2&4	5.542	55
28	28	1	51	O.OCO	5.542	55
29	29	1	52	0.224	5.542	55
3C	30	1	54	0.229	5.542	55
31	31	1	56	0.264	5.542	55
33	33	1	61	O.OCO	5.542	55
34	34	1	62	0.2*4	5.542	55
35	35	1	64	C229	5.542	55
36	36	1	66	e.c&o	5.542	55
42	42	1	61	0.394	5.542	55
43	43	1	£4	0.263	5.542	55
44	44	1	87	C096	5.542	55
45	45	1	a9	0.324	5.542	55
46	46	1	92	0.263	5.S42	55
48	48	1	98	0.263	5.542	55
51	52	1	1C6	0.096	5.542	55
52	52	2	108	C167	5.542	55
53	52	3	110	CU7	5.542	55
58	52	£	122	C096	5.542	55
59	52	9	124	COCO	5.542	55
to	S:	10	125	COCO	5.542	55
61	51	11	1 *Zi*	COCO	5.542	55
al	52	1Z	117	COCO	5.542	55
63	52	13	1*8	0.2*4	5.542	55
64	52	14	130	O.OCO	5.542	55
66	54	1	1 i!	0.2*9	5.542	55
71	59	1	1*7	C3i4	5.542	55

OUT OF 76 CANDIDATE TESTS 28 Afit KE"TA1*EO

Table 5.2 A5100 - Test Setup and Optimization Summary Report

5.4 NOPAL Specification and ATLAS Program Generation

The NOPAL specification for A5100 incorporating the above features has about 50 test modules, and 42 diagnoses. The listing is available separately in the accompanying documentation and computer tape, A short NOPAL specification to test the isolated single components is shown in Figure 5,6.

Because of the limitations of the memory size of the computer available for software development the bottom part of the NOPAL system is unable to generate one ATLAS program for the A5100 circuit. A temporary solution to the problem was to divide by hand the NOPAL specification for A5100 into four separate specifications. An interesting and encouraging observation was made here. The original circuit description contains two independent subcircuits: the monitor and the audio amplifiers. The original test specification easily divides into two disjoint parts (including the tests and their diagnoses) each relating to only one subcircuit. This behavior is not a coincidence. Any other behavior would have meant an erroneous specification. In the future, we are planning on exploiting this modularity property to speed the generation of specifications.

Various reports generated by the system makes it an easy task to split the specifications into several parts. The most useful tables are the test setup and logic optimization reports. In fact, a separate NOPAL specification can be generated for each diagnosis by simply including all the tests involved in selecting that diagnosis conjunctively. This would result in a large number of ATLAS programs. Instead several diagnoses referring to the desired -failures can be put together, and then all the tests required can be inserted into the specification. Then on

```
    /* NOPAL TEST SPECIFICATION SOURCE INPUT, FILE: SAPL1ST •/
1PAL PROCESSOR OPTIONS SPECIFIED: SAPLISTfNOXR£F1»CODE»SE«»6fNCXREF2,N0S0URCS2
IMT NO,

  1        NOPAL SPEC A5100;
        /************* * ***** ****************************************************/
  2        TEST CR51C3.SHORT;
  3         PEAS; CONJ:
  4             <A5 1_3, A51_5> * QHKMETERC >4QQE2, 400E3, 10E6, 2800);
  5          LOGIC: |* S.CR5103 ;
        /**************************************************************r**-*#********/
  6        TEST CR5103_CPEN;
  7         KEAS; CGNJ:
  8             <A51 5, A51 -3> * OHHHETERC < 4E3f 4E3, 39E3» 2800);
  9          LOGIC: Is Q.CR5103 ;
        /****************** *********************** ********** *************/
 10        TEST CR5104_SHORT;
 11         *£AS; CONJ:
 12             <A5i_1Qf A51_9> « OH««ETER( >4C0E3f 400E3, 10E6f Z8C0);
 13.         LOGIC: |" S.CR5104 ;
        /*********** **********************************************************/
 14        TEST CR51C4_CPEN ;
 15         *EA&; CONJ:
 U              <A51 9, A51_10> * OH««€TERC < 4£3f 4E3f 3963, 28C0);
 17          LOGIC: Is O.CR5104 ;
        /**************************************************************************/
 18        TEST R5117_CPEN ;
 19  •      HEAS; CONJ:
 2C             <A51 4f A51_6> * CH««£TERC RES_R5117, 1E3, Z.SBZ* 2800)
 20                   ~       TARGET: R6S.R5117;
 21          ASSERT: RES R5117 > 1760;
 22          LOGIC: I 0^5117;
        /**************************************************************************/
 21        TEST RS117_$H0RT;
 24         ffEAS;
 25          ASSERT: RES^R5117 < 1440;
 26          LOGIC: I S!R5117;
        /•*********** * ******* ***************** *************** ** ************/
 27        TEST C5108_CPEN ;
 28         PEAS; CONJ :
 29             <A51_6f SNO > * ZKETERC IMP_C5108, 1E3, 3.5E3,25C0, 8E3)
 29             TARGIT: I«P_C51C8;
 30          ASScRT: IKP C51G8 > 1760;
 31          LOGIC: / 0lc5108;
        /******** ********** ***** ** *****************************************/
 32        TEST C5108_SHORT;
 33         PEAS;
 34          ASSERT: IKP_C5108 < 1440;
 33          LOGIC: I Sj:51Q8;
        /**** **** *** * «*************************************************/
 36         DIA6 S_CR51C3: <SHCftT(Cfi5 1C3 ) * , FAIL.MSG);
 37         OIAfe o2cR51C3: <OPE»\( CR51 03 ) »t FAIL_MSG);
 38         OIAfa SICR51C4: (SHORT (C R5104) t, FAIL_MSG);
 39         OIAG O_CR51C4: (0PEN<CRi104) 9f FAIL.«SG);
```

Figure 5»6 NOPAL Specification For A5100-Subcircuits

```
40        DIAG O_R5117: (OPEN(R5117) ,, FAIL_MSG);
41        DIAG S_R5117: (SHORT(R5117) ,, FAIL_MSG);
42        DIAG O_C5108: (OPEN(C5108) ,, FAIL_MSG);
43        DIAG S_C5108: (SHORT(C5108) ,, FAIL_MSG);
      /*****************************************************************/
44        MESSAGE FAIL_MSG: TEXT= '***** FAILURE DETECTED - REPLACE (C) *****
      /*****************************************************************/
45        COMP_FAIL: CR5103, FAILURE=SHORT;
46        COMP_FAIL: CR5103, FAILURE=OPEN ;
47        COMP_FAIL: CR5104, FAILURE=SHORT;
48        COMP_FAIL: CR5104, FAILURE=OPEN ;
49        COMP_FAIL:  R5117, FAILURE=SHORT;
50        COMP_FAIL:  R5117, FAILURE=OPEN ;
51        COMP_FAIL:  C5108, FAILURE=SHORT;
52        COMP_FAIL:  C5108, FAILURE=OPEN ;
      /*****************************************************************/
53        FUNCTION: OPEN, TYPE=F;
54        FUNCTION: SHORT, TYPE=F;
55       FUNCTION: OHMMETER, FUNCTION TYPE = M, #PINS = 2,
55               PARAM_1 = (RESISTANCE, T REAL, LIMIT = (OHM, 10E6, 0)),
55               PARAM_2 = (MIN_RES, S REAL, LIMIT = (OHM, 10E6, 0)),
55               PARAM_3 = (MAX_RES, S REAL, LIMIT = (OHM, 10E6, 0)),
55               PARAM_4 = (REF_VOLT, S REAL, LIMIT = (MVOLT, 10E3, -10E3)),
55               COMMENTS = 'AUTORANGING OHMMETER';
56       FUNCTION: ZMETER, FUNCTION TYPE = M, #PINS = 2,
56               PARAM_1 = (CMPLX_IMP, T REAL, LIMIT = (OHM,  10E6, 0)),
56               PARAM_2 = (IMP_MIN,   S REAL, LIMIT = (OHM,  10E6, 0)),
56               PARAM_3 = (IMP_MAX,   S REAL, LIMIT = (OHM,  10E6, 0)),
56               PARAM_4 = (REF_VOLT,  S REAL, LIMIT = (VOLT,    7,    0)),
56               PARAM_5 = (FREQUENCY, S REAL, LIMIT = (HZ, 12.5E3, 10)),
56               COMMENTS = 'AUTORANGING COMPLEX IMPEDANCE METER';
      /*****************************************************************/
57        UUT_POINT : GND, CONNECTOR=(J8);
58        UUT_POINT : A51_3   , CONNECTOR=(J8);
59        UUT_POINT : A51_4   , CONNECTOR=(J8);
60        UUT_POINT : A51_5   , CONNECTOR=(J8);
61        UUT_POINT : A51_6   , CONNECTOR=(J8);
62        UUT_POINT : A51_9   , CONNECTOR=(J8);
63        UUT_POINT : A51_10  , CONNECTOR=(J8);
      /*****************************************************************/
64        END A5100;
RROR/WARNING MESSAGES GENERATED              DURING NOPAL SYNTAX ANALYSIS:
*STATISTICS* NO. OF SAP ERRORS =    0  ,   NO. OF WARNINGS =    0  , NO. OF S
ROR/WARNING MESSAGES GENERATED DURING CROSS-REFERENCE:
TATISTICS*  NO. OF XREF1 ERRORS =    0     NO. OF WARNINGS =    0
RROR/WARNING MESSAGES GENERATED DURING SEQUENCING AND CODE GENERATION:
RNING MESSAGES GENERATED DURING CODE GENERATION
ARNING* UUT POINT 'GND' NOT CONNECTED TO ANY ATE PIN
ARNING* UUT POINT 'A51-6' NOT CONNECTED TO ANY ATE PIN
ARNING* UUT POINT 'A51-4' NOT CONNECTED TO ANY ATE PIN
ARNING* UUT POINT 'A51-9' NOT CONNECTED TO ANY ATE PIN
ARNING* UUT POINT 'A51-10' NOT CONNECTED TO ANY ATE PIN
ARNING* UUT POINT 'A51-5' NOT CONNECTED TO ANY ATE PIN
ARNING* UUT POINT 'A51-3' NOT CONNECTED TO ANY ATE PIN
```

Figure 5-6 NOPAL Specification For A5100-Subcircuits (c

the ATE, any one of the programs can be run arbitrarily. If there is a failure, one of the programs will select the diag

This approach implies another interesting possibility. Fault diagnosis and fault isolation programs can be generat separately. The fault diagnosis program (containing only t nominal assertions) would indicate good or bad card only. card is bad, then the fault isolation programs could be run the ATE. During software testing phase of the research, th approach was taken to speed the ATE throughout.

5.5 Evaluation of EQUATE Runs

Figure 5.6 shows the NOPAL specification for testing t isolated components on the A5100 card. The execution of th ATLAS program generated for this specification is shown as third test run in Figure 5.7. Test sequence numbers and co points are documented inside the ATLAS program listing whic available separately. The failure detected by the program R5117 was actually due to a bad test point relay on EQUATE

When the same program was executed on EQUATE V, this f disappeared but another failure, short capacitor C5108, sho This was also a malfunction of the ATE, EQUATE V measured 0 complex impedance at and above 8KHertz.

The first two runs on Figure 5.7 are from an ATLAS pro which were generated from split NOPAL specifications. The run yields all nominal measurements. Test 11 refers to con points 255 and 200. These are not DIU points. When this t is invoked a message appears on the operator consolete givi instructions to connect high end of the probe to circuit no and the low end to ground (node 0). The failure detected i second run is a false alarm due to the resistance measureme

```
UUT: UP511.IC  REV: 12/14/79     DATE: 12/14/79  20:17:0

 TESTING UUT:  A5100
DATE 12/14/79 TIME 20:17: 1
TEST  1:      33.064 KOHM,  250 MV,   40 KOHM,  3 TIMES, CNX(22,41)
TE^^T  3:       1.546 KOHM,  250 MV,    4 KOHM,  2 TIMES, CNX(59,41)
TL .  6:  1.706 KOHM,-25 DEG, 1004 HZ, 1000 MV,   3.6 KOHM, 12 TIMES, CNX(41,:
TEST  9:  0.402 KOHM, -6 DEG, 1004 HZ, 1000 MV,   3.6 KOHM,  2 TIMES, CNX(41,5
TEST 11:        2.084 KOHM,  250 MV,    4 KOHM,  1 TIMES, CNX(255,200)
TEST 14:        0.372 KOHM,  250 MV,    4 KOHM,  1 TIMES, CNX(252,253)
TEST 16:     120.451 KOHM,  250 MV,  400 KOHM,  1 TIMES, CNX(255,254)
TEST 22:  0.000 KOHM,-44 DEG, 1004 HZ, 1000 MV,   3.6 KOHM,  1 TIMES, CNX(208,
UUT IS BEING POWERED NOW
TEST 20: APPLIED DC3A, 25.500 V, CNX HI 209 LO 200 .
        MEASURED 0.0015 AMPS THRU DC3A.
TEST 20: APPLIED DC2A, 16.000 V, CNX HI 202 LO 200 .
        MEASURED 0.0129 AMPS THRU DC2A.
TEST 20: APPLIED DC2B, 3.600 V, CNX HI 213 LO 200 .
        MEASURED 0.0061 AMPS THRU DC2B.


UUT: UP511.IC  REV: 12/14/79     DATE: 12/14/79  19:44:46

 TESTING UUT:  A5100
DATE 12/14/79 TIME 19:44:47
TEST  1:      32.980 KOHM,  250 MV,   40 KOHM,  3 TIMES, CNX(22,41)
TE^^T  3:       1.544 KOHM,  250 MV,    4 KOHM,  2 TIMES, CNX(59,41)
TL .  6:  1.694 KOHM,-24 DEG, 1004 HZ, 1000 MV,   3.6 KOHM,  7 TIMES, CNX(41,22
TEST  9:  0.403 KOHM, -6 DEG, 1004 HZ, 1000 MV,   3.6 KOHM,  5 TIMES, CNX(41,59
TEST 11:        2.080 KOHM,  250 MV,    4 KOHM,  1 TIMES, CNX(255,200)
TEST 14:        0.371 KOHM,  250 MV,    4 KOHM,  1 TIMES, CNX(252,253)
TEST 16:     120.311 KOHM,  250 MV,  400 KOHM,  1 TIMES, CNX(255,254)
TEST 22:  0.000 KOHM,-45 DEG, 1004 HZ, 1000 MV,   3.6 KOHM,  1 TIMES, CNX(208,2
POSSIBLE FAULTY COMPONENT(S) ---
BC-SHORT(QQ5101)          OR EC-SHORT(QQ5101)          OR SHORT(QDR5101)
UUT IS BEING POWERED NOW
JUT: UP51M.IC  REV: 12/14/79     DATE: 12/14/79  20:4:43

 TESTING UUT:  A5100
)ATE 12/14/79 TIME 20: 4:44
'EST  1: 176250.734 KOHM, 2800 MV, 1000 KOHM,  1 TIMES, CNX(43,37)
'EST  2:        1.825 KOHM, 2800 MV,   40 KOHM,  2 TIMES, CNX(37,43)
'EST  3:  36230.823 KOHM, 2800 MV, 1000 KOHM,  1 TIMES, CNX(34,61)
 EST  4:        2.013 KOHM, 2800 MV,   40 KOHM,  2 TIMES, CNX(61,34)
 EST  5:     677.064 KOHM, 2800 MV,    4 KOHM,  7 TIMES, CNX(44,38)
 **** FAILURE DETECTED - REPLACE OPEN(R5117) *****
 EST  7:  1.564 KOHM,-89 DEG, 8000 HZ, 2500 MV,   3.6 KOHM,  3 TIMES, CNX(38,41)
 INISHED TESTING AT 20: 6: 5
 JRATION   0: 1:21
 ) YOU WISH TO SEE THE FINAL FAULT ISOLATION STATE ? (Y/N)
 ) YOU WISH TO RERUN THIS PROGRAM? (Y/N)
```

Figure 5.7 NOPAL Printouts For A5100 Subcircuits

UUT: UP5U. 1C REV: 11/2/79 DATE: 11/2/7? 20:2:21

```
 TESTIMG UUT:
DATE 11/ 2/79 TIME 20: 2::22
TEST  1:     32. 909 KOHM,  250 MV,    40 KOHM, 2 TIMES, CNX(22, 41)
TEST  2:      1. 572 KOHM*  250 MV,     4 KOHM, 2 TIMES, CNX (59,41)
TEST  3: 1763S. 283 KOHM,   250 MV,   400 KOHM, 4 TIMES, CNX(47, 41)
TEST  3: 10665. 117 KOHM,   250 MV*  1000 KOHM, 14 TIMES* CNX(47* 41)
TEST  4:      0. 154 KGHM*  250 MV,     4 KOHM, 2 TIMES, CNX(48, 41)
TEST  5: 89981. 338 KQHM*   250 MV,   400 KOHM, 1 TIMES, CNX(61, 41)
TEST  5: 10930S. 650• KOHM*  250 MV,  1000• KOHM, 2 TIMES, CNX (61, 41)
TEST  6:      0. 432 KOHM,  250 MV,     4 KOHM, 2 TIMES, CNX(33* 41)
TEST  7: 72552. 555 KOHM,   250 MV*   400 KOHM, 1 TIMES, CNX(24* 41)
TEST  7: 95795. 853 KQHM,   250 MV,  1000 KOHM, 2 TIMES* CNX<24* 41)
TEST  S:     SI. 1S4 KOHM,  250 MV,   400 KOHM, 13 TIMES, CNX(25*41)
TEST  9:     34. 530 KOHM,  250 MV,    40 KOHM, 5 TIMES, CNX(59, 22)
TEST 10: 24494. 642 KOHM,   250 MV,   400 KOHM, 4 TIMES, CNX(47* 22)
TEST 10: 10142. 093 KOHM,   250 MV,  1000 KOHM, 14 TIMES, CNX(47* 22)
TEST 11:     33. 053 KOHM.  250 MV,    40 KOHM, 10 TIMES, CNX(48, 22)
TEST 12: 132603. 902 KOHM,  250 MV,   400 KOHM, 1 TIMES, CNX(61* 22)
TEST 12: 107595. 991 KOHM,  250 MV,  1000 KOHM* 2 TIMES* CNX(61, 22)
TEST 13:     33. 203 KOHM,  250 MV,    40 KOHM, 3 TIMES, CNX(33, 22)
TEST 14: 797S90. 9S6 KOHM*  250 MV,   400 KOHM, 1 TIMES, CNX(24* 22)
TEST 14: 134439. 442 KOHM,  250 MV,  1000 KOHM, 2 TIMES* CNX(24*22)
TEST 15:     92. 510 KOHM*  250 MV,   400 KOHM, 13 TIMES, CNX(25, 22)
TEST 16: 10709. 460 KOHM,   250 MV,   400 KOHM, 3 TIMES, CNX(47* 59)
TEST 16: 10428. 643 KOHM,   250 MV,  1000 KOHM, 12 TIMES, CNX(47, 59)
TEST 17:      1. 726 KOHM,  250 MV,     4 KOHM, 2 TIMES, CNX(43, 59)
TEST IS: 292449. 814 KOHM*  250 MV,   400 KOHM, 1 TIMES, CNX(61* 59)
TEST IS: 115824. 900 KOHM,  250 MV*  1000 KOHM, 2 TIMES, CNX(61* 59)
TEST 19:      2. 050 KOHM,  250 MV,     4 KOHM* 2 TIMES* CNX(33* 59)
TEST 20: 117108. 331 KOHM,  250 MV,   400 KOHM, 1 TIMES, CNX(24, 5?)
TEST 20: 188795. 573 KOHM,  250 MV,  1000 KOHM, 2 TIMES, CNX(24,5?)
TEST 21:     79. 124 KOHM,  250 MV,   400 KOHM, 12 TIMES, CNX(25* 59)
TEST 22: 12046. 924 KOHM,   250 MV,   400 KOHM, 5 TIMES, CNX(48* 47)
TEST 22* 10706. 993 KOHM*   250 MV*  1000 KOHM, 14 TIMES* CNX(48* 47)
TEST 23: 295231. 104 KOHM,  250 MV,   400 KOHM, 1 TIMES, CNX (61,47)
TEST 23: 49S060. 784 KOHM,  250 MV,  1000 KOHM, 2 TIMES, CNX(61,47)
**** GOOD UUT •••*
FINISHED TESTING AT 20:10:50
DURATION   0:8:23
DO YOU WISH TO SEE THE FINAL FAULT ISOLATION STATE ? (Y/N)
DO YOU WISH TO RERUN THIS PROGRAM? <Y/N)
TERHINATE EQUATE PROGRAM -'A5100-1'
```

Figure 5.7 NOPAL Printouts For A5100 Subcircuits (conti

```
UUT: UP512.IC  REV: 11/2/79      DATE: 11/2/79  20:14:7

  TESTING UUT:  A5100-2
DATE 11/ 2/79 TIME 20:14: 7
TEST  1: 14919.502 KOHM,  250 MV,  400 KOHM, 4 TIMES, CNX(33,47)
TEST  1: 11598.958 KOHM,  250 MV, 1000 KOHM, 15 TIMES, CNX(33,47)
TEST  2: 943503.348 KOHM,  250 MV,  400 KOHM, 1 TIMES, CNX(24,47)
TEST  2: 98167.027 KOHM,  250 MV, 1000 KOHM, 2 TIMES, CNX(24,47)
TEST  3: 11687.993 KOHM,  250 MV,  400 KOHM, 7 TIMES, CNX(25,47)
TEST  3: 10787.617 KOHM,  250 MV, 1000 KOHM, 19 TIMES, CNX(25,47)
TEST  4: 356212.721 KOHM,  250 MV,  400 KOHM, 1 TIMES, CNX(61,48)
TEST  4: 225281.575 KOHM,  250 MV, 1000 KOHM, 2 TIMES, CNX(61,48)
TEST  5:      0.635 KOHM,  250 MV,    4 KOHM, 2 TIMES, CNX(33,48)
TEST  6: 124624.512 KOHM,  250 MV,  400 KOHM, 1 TIMES, CNX(24,48)
TEST  6: 92530.249 KOHM,  250 MV, 1000 KOHM, 2 TIMES, CNX(24,48)
TEST  7:     71.553 KOHM,  250 MV,  400 KOHM, 15 TIMES, CNX(25,48)
TEST  8:    211.051 KOHM,  250 MV,  400 KOHM, 4 TIMES, CNX(33,61)
TEST  9:      0.089 KOHM,  250 MV,    4 KOHM, 2 TIMES, CNX(24,61)
TEST 10: 94832.163 KOHM,  250 MV,  400 KOHM, 3 TIMES, CNX(25,61)
TEST 10:    564.010 KOHM,  250 MV, 1000 KOHM, 5 TIMES, CNX(25,61)
TEST 11: 175251.528 KOHM,  250 MV,  400 KOHM, 1 TIMES, CNX(24,33)
TEST 11: 150589.136 KOHM,  250 MV, 1000 KOHM, 2 TIMES, CNX(24,33)
TEST 12:     73.392 KOHM,  250 MV,  400 KOHM, 24 TIMES, CNX(25,33)
TEST 13: 11818.675 KOHM,  250 MV,  400 KOHM, 3 TIMES, CNX(25,24)
TEST 13:    564.921 KOHM,  250 MV, 1000 KOHM, 6 TIMES, CNX(25,24)
TEST 14: IMPEDANCE 1623.6 OHM, -24.9 DEG, 1.0 KHZ, REF-VOLTAGE 1000 MV,
         ITERATED 1 TIMES, CNX HI 41 LO 22 .
TEST 15: IMPEDANCE 415.9 OHM, -6.6 DEG, 1.0 KHZ, REF-VOLTAGE 1000 MV,
         ITERATED 1 TIMES, CNX HI 41 LO 59 .
TEST 16: IMPEDANCE 144.6 OHM, -0.3 DEG, 1.0 KHZ, REF-VOLTAGE 1000 MV,
         ITERATED 1 TIMES, CNX HI 41 LO 48 .
TEST 17: IMPEDANCE 2035.8 OHM, -27.6 DEG, 1.0 KHZ, REF-VOLTAGE 1000 MV,
         ITERATED 1 TIMES, CNX HI 41 LO 25 .
TEST 18: IMPEDANCE 77.0 OHM, -12.1 DEG, 1.0 KHZ, REF-VOLTAGE 1000 MV,
         ITERATED 1 TIMES, CNX HI 47 LO 59 .
TEST 19: IMPEDANCE 2498.1 OHM, -24.4 DEG, 0.1 KHZ, REF-VOLTAGE 100 MV,
         ITERATED 1 TIMES, CNX HI 41 LO 22 .
TEST 20: IMPEDANCE 423.4 OHM, -7.3 DEG, 0.1 KHZ, REF-VOLTAGE 100 MV,
         ITERATED 1 TIMES, CNX HI 41 LO 59 .
TEST 21: IMPEDANCE 144.6 OHM, 0.6 DEG, 0.1 KHZ, REF-VOLTAGE 100 MV,
         ITERATED 1 TIMES, CNX HI 41 LO 48 .
TEST 22: IMPEDANCE 2127.6 OHM, 4.4 DEG, 0.1 KHZ, REF-VOLTAGE 100 MV,
         ITERATED 1 TIMES, CNX HI 41 LO 25 .
TEST 23: IMPEDANCE 183.5 OHM, -64.1 DEG, 0.1 KHZ, REF-VOLTAGE 100 MV,
         ITERATED 1 TIMES, CNX HI 47 LO 59 .
FINISHED TESTING AT 20:22: 8
DURATION   0: 8: 1
DO YOU WISH TO SEE THE FINAL FAULT ISOLATION STATE ? (Y/N)
DO YOU WISH TO RERUN THIS PROGRAM? (Y/N)
TERMINATE EQUATE PROGRAM 'A5100-2'
```

Figure 5.7 NOPAL Printouts For A5100 Subcircuits (cc

across diode CR5101. The simulation results expected very l
resistance (> 400 Kohm). However test equipment measured
approximately 120 Kohm. Such a large discrepency is due to
inaccurate EBERS-MOLL model of the transistor and diode at v
low current levels. Unfortunately, this is a case which re
a change in the semiconductor model to remove the inaccuracy

The last two runs illustrate the performance of a diagn
program which contains only nominal assertions. The output
A5100-1 shows that upon the completion of all test the UUT i
found to be nominal under the tests conducted so far. The c
labelled A5100-2 does not contain a "nominal UUT" message.
this case, the problems arose from the fact that the EQUATE
make accurate impedance measurements when the reference volt
is less than one volt. This poses a serious problem in circ
simulation because ac circuit behavior is simulated utilizin
small-signal response where linearity is assumed at levels v
close to the operating point. Higher voltage levels (such a
start pushing the semiconductors to their conducting and non
conducting ranges during the application of the sinusoidal i
This problem can best be alleviated by removing the line-vol
modulation which is present on the floating ac-standard sign
(approximately 0.2 volts) on the EQUATE.

CHAPTER VI

Conclusion

In the course of the research it was decided that no major changes to the NOPAL system should be done to highlight and understand the deficiencies and successful aspects of the current implementation. In our view this rigidity was necessary at this time because there is no other methodology (manual or automatic) which can be compared to NOPAL to determi its effectiveness. Hence this version of NOPAL will serve as a baseline for our future developments. During the past year minor changes which do not conflict with the concept of NOPAL were introduced. Because these changes are minor and do not influence the operation of the algorithm a separate documentation for the system is not required.

The NOPAL system has been used to generate specifications diagnose and isolate the failures in two analog circuit cards. Portions of these specifications were used to generate many short ATLAS programs to test for specific failures. As the research progressed, it was found that the NOPAL concept of automatic programming indeed works well as intended. That is, once a circuit description is available, the generation of ATLAS programs and the specification of tests for a given circuit can be done completely automatically. However, occasionally it may be necessary to evaluate the intermediate results to understand the progress of program generation.

Because the only input to the system is the circuit description of the card to be tested, the accuracy of the models used in the input becomes the most critical component of the process. This is especially important in the case of semiconductors. When a technician tests, say a diode, several hundred percent tolerance on its reverse impedance would pass his inspection. However, in the case of circuit component modelling this tolerar must be specified precisely, or else the NOPAL system may put the go-nogo limits in ranges which result in a large number of false alarms.

The following comments identify some problem areas which need further investigation:

1. A laboratory type setup to verify the published semiconduct models is required. If the models have not been previously published, a facility to develop circuit analysis models is needed. This would reduce the chances of unsuccessful ATE runs due to wrong component modelling,

2. The ATLAS programs generated by NOPAL tend to be several thousand statements long. The EQUATE executes ATLAS statements very slowly. The code should be optimized. For example, if the programs execute the test performance logic of the fault isolation tree, the programs would run faster.

3. In many cases the specifications generated become very lengthy. It becomes a serious problem to generate partial programs. The NOPAL system can be modified such that it generates several programs, if it becomes impossible to fit it all at once into memory.

4. Circuit simulation time can be reduced significantly by taking advantage of circuit topology and failure definition

5. When the tests performed at the available test points do nc result in satisfactory fault isolation levels, the NOPAL system may automatically select a minimum number of manually probed test points.

6. Finally the test selection strategy should be improved and designed to operate in ranges where the ATE is most accurate. The designer should be warned if any test is selected where the accuracies of the stimulus and measurement are marginal according to the ATE performance specification•

7, Tests which result in long delays, such as resistance measurement across capacitive loads, should be avoided. Such cases should be found by circuit simulation and replaced by appropriate impedance measurements.

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APPENDIX

1. Diode and Zener Diode Models
   1N645, 1N4001, 1N752A

2. Transistor Models
   ZN329A, 2N335, 2N404A

```
internal node I is the cathode
CURGEN/EXP/    A       -0.25100E-09   B        0.25100E-09   >
               D        0.33314E-01    L   -2.00    U    0.10
DIF   /    /   B        0.12500E-03    C       -0.25100E-09
TRAN  /    /   B        0.10600E-10    C    0.26    D    -1    E      -0.57
S    1    2           0.12300E 09
D    1    2     1*CURGEN(VID)
T    1    2      1*CTRAN(VID)
D    1    2    1*CDIF(IID)
B     2     3           0.53200E-03


32     D1N4001 +
TERNAL NODE 1 IS THE ANODE
TERNAL NODE 3 IS THE CATHODE
GEN/EXP/    A      -0.80000E-08   B        0.80000E-08   >
            D        0.47619E-01    L   -0.20    U    0.80
F   /   /   B       0.24000E-04    C       -0.80000E-08
AN   /   /  B       0.13000E-10    C    1.00    D    -1    E      -0.4100(
  1    2          0.64000E+09
  1    2     1*CURGEN(VID)
  1    2      1*CTRAN(VID)
  1    2    1*CDIF(IID)
   2     3        0.10000E+00


     Z1N752A  +
N/EXP/  A     -0.125E-10    B     0.125E-10   >
        D      0.32468E-01  L   -2.0   U    0.8
P/TAB2/  -3.0        -10.0        >
         -1.0         -6.0        >
         -0.8         -0.5        >
         -0.6        -0.05        >
         -0.5        -0.2E-02     >
         -0.4?       -0.1E-06     >
          0.0         0.1E-08     >
          1.0         0.1E-05     >
          4.9         0.1E-05     >
          5.2?        0.1E-02     >
          5.34          .02         >
          5.41          .05
    /    B     0.31E-05     C     -0.125E-10
    /    B     0.373E-09    C      0.75     >
         D      -1.0        E     -0.5
  1   2     0.157
  2    1     1*CURGEN(VID)
  1    2     1*ZENCUR(VIZ)
  2    1     1*CTRAN(VID)
  2    1     1*CDIF(VID)
  2    3     11
```

```
.IB2      TR2N3Z9A   +
MTRAN/  /  B      0.28000E-10       C      0.8    D    -1    E      -0.470
EMTRAN.B IS CONSTANT OF THE EMITTER  TRANSITION CAPACITANCE (COE)
EMTRAN.C IS EMITTER BASE JUNCTION CONTACTPOTENTIAL (FIE)
EMTRAN.D  IS  -1
EMTRAN.E IS NEGATIVE OF EMITTER JUNCTION  GRADING CONSTANT  (-NE)
ITCUR/EXP/  A     -0.21600E-13    B          0.21600E-13  D  0.25641000E
MTCUR.A IS NEGATIVE OF EMITTER BASE SATURATION CURRENT  >
                         MEASURED IN THE ACTIVE REGION
 MTCUR.B IS EMITTER BASE SATURATION CURRENT MEASURED IN  >
                             THE ACTIVE REGION
 MTCUR.D IS THE INVERSE OF CONSTANT OF EMITTER  BASE JUNCTION  >
                             EQUATION (VTE)
 TDIF/    /  A       0.21600E-13
 LDIF/     /   A        0.62200E-10
 LLCUR  /EXP/  A      -0.62200E-10  B      0.62200E-10  D        0.3448
OLLCUR.A IS NEGATIVE OF COLLECTOR BASE   SATURATION CURRENT  >
              MEASURED IN THE ACTIVE REGION
OLLCUR.B IS THE COLLECTOR BASE SATURATION   CURRENT >
               MEASURED IN THE ACTIVE REGION
OLLCUR.D IS THE INVERSE OF CONSTANT OF  COLLECTOR BASE JUNCTION  >
                             EQUATION (VTC)
 RAN/ /  B      0.96000E-10 C       0.80000E 00   D  -1   E      -0.5000
.TRAN.B IS CONSTANT OF THE COLLECTOR TRANSITION  CAPACITANCE  >
                              EQUATION (COC)
.TRAN.C IS COLLECTOR BASE JUNCTION CONTACT   POTENTIAL (FIC)
.TRAN.D IS -1
 TRAN.E IS NEGATIVE OF COLLECTOR JUNCTION  GRADING CONSTANT (-NC)
    2     4     350.00000 :BASE BULK RESISTANCE
     4      3        0.50000E 08 :EMITTER BASE JUNCTION LEAKAGE RESISTAN
     3      4      1*EMTCUR(VIE)
    4      3     1*EMTRAN(VIE)
 P1=     0.39000E 02*     0.88000E-07
 MP2 = 1* EMTDIF(IIE)
     4      3      1*PTEMP1*PTEMP2
    4      5         0.97200E 00  IIE
    4      5        0.50000E 08 :COLLECTOR BASE  JUNCTION LEAKAGE RESISTA
    5       4      1*COLLCUR(VIC)
    4      5    1*CLTRAN(VIC)
 MP3=     0.29001E 02*     0.14000E-04
 MP4 =  1*COLDIF(IIC)
      4      5      1*PTEMP3*PTEMP4
    4      3       0.86000E 00 IIC
    5      1          0.32000E 02 :COLLECTOR BULK RESISTANCE
```

```
LI-5 2      TR<.HZ:5      •
•\TKA\/    /    o       C.51CCrg-1j       C       !•£'    i>     -1     E       -G.43QI
£VTRA^.5 IS CON?TA;*T OF THc EMITTEK  TRANSITION CAPACITANCE (COE)
ƨViTPA^.C  IS  cYITTE^  BASE JUNCTION CONTACTP0T£NTIAL  (FIE)
L^TP^.O     15     -1
:VTSA>*.S  IS  NEGATIVE  OF  EMITTEK  JUNCTION   GRADING  CONSTANT   (-NE)
MTCUR/CX?/   A      -T.4t03d-.12     2          :.4S433E-12   D   0.?37c3990E
i^TCJR.A  IS  NEGATIVE  OF  EMITTER  &ASE  SATURATION  CURRENT   >
                         MEASURED  IN  THE  ACTIVE  REGION
L*TCJ3.3  IS  E1ITTER 5ASB SATURATION CURRENT MEASURED  IN   >
                            TH£  ACTIVE  REGION
·VTCJ?.D  IS  TH£  IWESSd  OF  CONSTANT  OF  EMITTER   3ASE  JUNCTION   >
                            EQUATION  (VTE)
 TDIF/     /    A          0.4?430E-12
 L^IF/      /     A           Ct27i3GE-11
 LLCJ^J   /EXP/   :        -C.27S30E-11   B        C.27800E-11    D          C.337S
 CLLCJK.A  IS  NEGATIVE  CF  COLLECTOR  5AS£    SATURATION  CURRENT   >
               Mc^SURSD  IN  THE  ACTIVE  REGION
 CLLCJR.J  IS  THE  COLLECTOR  3AS£  SATURATION    CURRENT >
                KEASUPEO  IN  The  ACTIVE  REGION
 OLLC'JR.D  IS  Tht  INVERSE  OF  CONSTANT  OF   COLLECTOR  BASE  JUNCTION   >
                            EQUATION  (VTC)
 THĤH/  /   't          :.1QCCO£-1D  C        0..CC030E  OQ    D   -1   £        -3.323:
 LTR*M.3  IS  CONSTANT  CF  THE  COLLbCTOH  TRANSITION   CAPACITANCE   >
                             EQUATION  (COO
 ,T?*>4.C  IS  COLLECTOR  6ASE  JUNCTION  CONTACT    POTENTIAL  (FIC)
 .TRAN.D  IS  -1
 .TR'^.E  IS  NEGATIVE  OF  COLLECTOR  JUNCTION   GRADING  CONSTANT  (-NC)
    I      t>      3C5•CCCCC  :BAS£  SULK  RESISTANCE
     ^       2        U.5CCC0E  3b  :SMITTER ??ASE JUNCTION L£ANAGE RESISTAN
     ^       3        1«E>ITCU« (VIE)
    4        3        1*EMTRAN(VIE)
 !F1=        0.296U2c  :2*      3.615CCE-0?
 MP2  =  1*  E^TDTF CUE).
    4      i        1*PTE*P1*PT£*P2
    5       4          3.98irOE  30   HE
    4      5          C.53CC3E  C£  COLLECTOR  2ASE   JUNCTION  LEAKAGE  RESIST-
    4       5       1*C0LLCUfi(VIC)
    4      5       1*CLT9AN (VIC)
 MP3=      0.4?6?CE  C2*      i.46GCCE-2fc
 MP4  =    1*C0LüIF (IIC)
     4       5       1 *PT£*!P3*Pf EXP4
    3       *.       J.5CC30E  30   IIC
    5       1          C.esCQGE 02  :COLLECTOR £UL< RESISTANCE
```

```
NTERNAL NODE 1  IS COLLECTOR
NTERNAL NODE 2  IS BASE
NTERNAL NODE 3  IS EMITTER
TRAN/  /  B      0.15600E-10       C      1.2   D   -1   E      -0.5900
MTRAN.B IS CONSTANT OF THE EMITTER  TRANSITION CAPACITANCE (COE)
MTRAN.C IS EMITTER BASE JUNCTION CONTACTPOTENTIAL (FIE)
MTRAN.D  IS  -1
MTRAN.E IS NEGATIVE OF EMITTER JUNCTION  GRADING CONSTANT  (-NE)
TCUR/EXP/  A     -0.20300E-04    B         0.20300E-04  >
                        D  0.42918440E-01     L  -8.0    U   0.7
MTCUR.A IS NEGATIVE OF EMITTER BASE SATURATION CURRENT  >
                    MEASURED IN THE ACTIVE REGION
MTCUR.B IS EMITTER BASE SATURATION CURRENT MEASURED IN  >
                       THE ACTIVE REGION
MTCUR.D IS THE INVERSE OF CONSTANT OF EMITTER  BASE JUNCTION  >
                       EQUATION (VTE)
TDIF/   /  A       0.20300E-04
LDIF/     /   A       0.21400E-04
LLCUR  /EXP/  A     -0.21400E-04  B       0.21400E-04  >
                        D  0.45662110E-01     L  -8.0    U   0.7
OLLCUR.A IS NEGATIVE OF COLLECTOR BASE   SATURATION CURRENT  >
            MEASURED IN THE ACTIVE REGION
OLLCUR.B IS THE COLLECTOR BASE SATURATION   CURRENT >
             MEASURED IN THE ACTIVE REGION
OLLCUR.D IS THE INVERSE OF CONSTANT OF  COLLECTOR BASE JUNCTION  >
                       EQUATION (VTC)
TRAN/ /  B      0.56600E-10 C        0.31300E+01  D  -1  E      -0.826
LTRAN.B IS CONSTANT OF THE COLLECTOR TRANSITION  CAPACITANCE  >
                        EQUATION (COC)
LTRAN.C IS COLLECTOR BASE JUNCTION CONTACT   POTENTIAL (FIC)
LTRAN.D IS -1
LTRAN.E IS NEGATIVE OF COLLECTOR JUNCTION  GRADING CONSTANT (-NC)
   2    4       1.90000 :BASE BULK RESISTANCE
    4     3       0.64700E+07 :EMITTER BASE JUNCTION LEAKAGE RESISTA
    4     3      1*EMTCUR(VIE)
T  4     3     1*EMTRAN(VIE)
EMP6=       0.23300E+02
EMP1=     0.28600E-06*PTEMP6
EMP2 =  1*EMTDIF(IIE)
    4     3     1*PTEMP1*PTEMP2
   5     4        0.98400E+00  IIE
   4     5        0.74600E+07 :COLLECTOR BASE  JUNCTION LEAKAGE RESIST
   4     5     1*COLLCUR(VIC)
T  4     5    1*CLTRAN(VIC)
EMP7=     0.21900E+02
EMP3=     0.34900E-05*PTEMP7
MP4 =   1*COLDIF(IIC)
    4      5       1*PTEMP3*PTEMP4
   3     4        0.93000E+00 IIC
   5     1         0.10000E+00 :COLLECTOR BULK RESISTANCE

N
D
```