A RELIABILITY MODEL FOR VARIOUS SWITCH DESIGNS IN HYBRID REDUNDANCY

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ABSTRACT

Various switch designs for the hybrid redundancy scheme are studied. A reliability model for the switch is developed and the switch is shown to be a significant factor in the overall system reliability. A hybrid redundancy scheme with a triple-modular redundant (TMR) core may have a maximum attainable reliability for only a spare or two. Adding spares complicates the switch enough to cause the system reliability to actually decrease. There exist conditions under which the switch becomes so complex that simple TMR would yield a better solution. Models for fault-tolerant switch designs are also obtained. Finally, various designs are compared via their reliability models.

Key Phrases - Triple modular redundancy (TMR), hybrid redundancy, checker-redundant scheme, quadded logic, radial logic, mission time improvement (MTI).

INTRODUCTION

The advent of relatively inexpensive LSI technology and the increasing demand for fault-free operation of digital systems for long periods of time have rekindled the interest in fault tolerant computer design. In order to predict the performance of a particular design or compare two or more designs, an accurate reliability model is needed.

In this paper we will discuss various switch designs for the hybrid redundancy scheme [MathF70]. It will be shown that the switch reliability is an important factor in determining the overall system reliability. The current effort is directed towards obtaining a suitable model for the switch designs. A model will be presented and it will be used to compare the various designs. First we will present the redundancy schemes to be studied.

REDUNDANCY SCHEMES

Hardware redundancy may be used in a variety of manners to achieve fault tolerance. Among the best known techniques are the replication schemes, such as triple modular redundancy (TMR) and N-modular redundancy (NMR). TMR, first proposed by Von Neumann [VonNJ56], divides a nonredundant circuit into modules and replicates each module thrice. A majority voter is used on the outputs of the triplicated modules (Fig. 1a). Such a scheme has also been referred to as masking redundancy because failures that affect only one of the three modules are "masked" by the majority of the nonfailed modules. Since the scheme can tolerate one module failure without a system failure, the reliability of the

system in Fig. 1a may be written in terms of the module reliability, R, and the voter reliability, R_v, as

$$R_{TMR} = R_v \cdot \{ R^3 + 3 R^2 (1-R) \} \qquad (1)$$

$$= R_v \cdot \{ 3 R^2 - 2 R^3 \}$$

Note that this equation and all the equations that follow assume the classical reliability model, namely, that once a module has failed its output is assumed to always be in error.

NMR is a logical extension of TMR for any odd number N. If $N = 2t + 1$, the NMR system of Fig. 1b can tolerate as many as t module failures. The reliability of such a system is, therefore,

$$R_{NMR} = R_v \cdot \{ \sum_{i=0}^{t} \binom{N}{i} R^{N-i} (1-R)^i \} \qquad (2)$$

Hybrid redundancy has been proposed [MathF70], [GoldJ66] as a means to achive reliability and longer times of fault-free operation than those attainable by TMR or NMR systems. Fig. 2 shows a hybrid redundancy scheme. The switching network is used to select three of the m modules, whose outputs are to be voted on. These modules form a TMR core. Faulty modules are detected by comparing module outputs to the voter output. A faulty module in the TMR core is logically replaced by one of the spares that have not yet failed. If only one of the three TMR core modules is assumed to fail at a time, the system fails only if all the modules fail or if all but one module fail. The reliability of the hybrid system with a TMR core and m-3 spares is

$$R_{HYB} = R_v \cdot R_{sw} \cdot \{ 1 - mR(1-R)^{m-1} - (1-R)^m \} \qquad (3)$$

where R_{sw} is the reliability of the switch.

Again, a hybrid scheme with a TMR core may be extended to one with an NMR core. In the current discussion, we will implicitly refer to a hybrid scheme

with a TMR core as the hybrid system. Thus, although the treatment that follows is only that of a particular case, it may easily be extended to any N other than 3.

Since a three input voter will appear in all the redundancy schemes to be discussed, the voter reliability, R_v, in the expressions for system reliability will be identical for all the schemes. As the focus of the discussion to follow will be on comparison of schemes, the constant multiplying term R_v, may be omitted without affecting the analysis.

Another scheme that will be discussed has been proposed by [RamaC73]. In this scheme, referred to as the checker-redundant scheme (Fig. 3), every module is associated with a checker. Only one module is active at a time, and it is replaced by another if its checker detects a fault. The system fails only if all modules fail. The reliability of a checker redundant scheme with m modules is

$$R_{CRS} = R_{SW} \cdot \{ 1 - (1 - R.R_{ch})^m \} \qquad (4)$$

where R_{ch} is the reliability of a checker.

It has been a common practice in the past either to assume the switch to be ultra-reliable ($R_{SW} = 1$) or to assume its reliability to be independent of the total number of modules in the hybrid scheme. Under this assumption, the system reliability can be improved simply by adding more modules. For the hybrid scheme, subtracting the system reliability for m modules from that for m+1 modules, we get

$$R_{SW} .(1-(m+1).R(1-R)^m-(1-R)^{m+1}) - R_{SW} .(1-mR(1-R)^{m-1}-(1-R)^m) \qquad (5)$$

$$= R_{SW} \cdot mR^2(1-R)^{m-1}$$

This expression is positive for any $0 < R < 1$ and $m \geq 1$. Therefore, under the

assumption that R_{SW} is independent of m, adding modules increases the system reliability.

It is easily seen from (4) that under the assumption that R_{SW} is independent of m, R_{CRS} can also be increased by simply increasing m.

In the discussion to follow, a more realistic model for the switch reliability will be presented. Various schemes to improve the switch reliability will also be considered. The TMR scheme will be used as a basis for comparison of the schemes. Results will be compared with the experimental work presented by [OgusR73].

A MODEL FOR THE SWITCH

The switch required for hybrid redundacy has been the subject of recent research. [SiewD73a] discussed switching strategies. In [SiewD73b], an iterative cell switch for hybrid redundancy was prsented. [OgusR73] presented some techniques to improve fault-tolerance of the voter, switch and disagreement detector.

The current discussion will attempt to explore the switch in detail. An effort is made towards achieving a close analytical model for the switch.

In order to facilitate concise presentation, it is appropriate that some terms be defined at this point. The symbol R will be used for the reliability of the basic module. R_{SYS} will be used for the system reliability and m for the number of modules in the system. As is customary, it will be assumed that each module has passed through an extensive burn-in period. This allows us to assume that R is an exponential function of time with a constant failure rate, λ, i.e. $R = e^{-\lambda t}$. R_{SW} will be used for the reliability of the switch and the symbol R

with appropriate subscripts will be used to denote the R_{sys} of a scheme under consideration.

We have already seen that R_{sys} for both the hybrid and the checker redundant schemes increases with m under the assumption that R_{sw} is independent of m. This assumption, however, is questionable. It is only to be expected that the switch will become more complex as more modules are added. The actual dependance of the switch complexity on m will be a function of the particular design. In the switch designs that were studied, the complexity, evaluated in terms of the number of gates and the number of states that a switch is required to assume, was found to be nearly linearly dependent on m, that is, the addition of each module to the system increased the switch complexity by a constant amount. The designs included a switch for the hybrid scheme as well as other systems such as a byte-oriented reconfigurable memory system. An iterative cell design for the hybrid scheme [SiewD73b] also supports this assertion. Fig. 4 shows the iterative cell design for a hybrid scheme with a TMR core and two spares. An additional spare will require extra hardware equal to that in the box shown with a dotted line in Fig. 4. Consequently, as a more realistic assumption, we will consider the R_{sw} to be p^m, where p is the reliability of the switch component which must be added when a module is added. This is based on the assumption that the switch complexity grows linearly with m. In the iterative cell design, p would be the reliability of the hardware in the box in Fig. 4. The expression, p^m, will be modified to suit the particular redundancy scheme being considered.

NEW MODELS

We will now introduce two parameters, α and β. These will be used to relate the reliabilities of the switch and the checker, respectively, to R. We will let $p = R^{\alpha}$ and $R_{ch} = R^{\beta}$. Thus, α and β are the measures of how complex the incremental switch component and the checker are compared to the basic module. The system reliabilities for the hybrid system of Fig. 2 and checker redundant scheme of Fig. 3 may be rewritten as

$$R_{HYB} = R^{m\alpha}.\{ 1 - m(1-R)^{m-1}R - (1-R)^{m} \} \tag{6}$$

$$R_{CHS} = R^{m\alpha}.\{ 1 - (1-R^{1+\beta})^{m} \} \tag{7}$$

COMPARING SCHEMES

Before we enter the discussion of various schemes, we must develop the measures for evaluation and comparison of the schemes. R_{sys} is the most obvious measure. As will be evident from the examples that will be presented, the graphs of R_{sys} against m effectively bring out the dependance of R_{sys} on m as a result of the dependance of R_{sw} on m. However, for comparing systems that are highly reliable, R_{sys} is of little value.

Another absolute measure that may be used is the mission time. The mission time, t_m, is defined to be the time at which R_{sys} is exactly equal to some pre-determined value. It is, in other words, the time after which R_{sys} drops below that required for the minimum desirable performance. Given R_{sysmin}, the minimum system reliability desired, t_m may be determined by using $R_{sys}(t_m) = R_{sysmin}$.

A more interesting measure, and one that will be used extensively in the examples that follow, is a comparative one, namely, the *M*ission *T*ime

*I*mprovement (MTI). MTI is defined to be the ratio of the mission times of the two schemes to be compared. It is more useful measure because MTI may be determined without specifying R_{sysmin}, which may depend on various system requirements. If for schemes 1 and 2, $R_{sys1}(t_1) = R_{sys2}(t_2)$, then the MTI of scheme 1 over scheme 2 is (t_1/t_2). If the two schemes have modules with identical failure rates λ, with $R_1 = e^{-\lambda t}$ and $R_2 = e^{-\lambda t}$, the MTI also equals $(ln\ R_1/ln\ R_2)$.

The relative complexity of the switch, α, may also be considered a measure for evaluation. It may be used as both an absolute and a relative measure. The α required for the m which optimizes R_{sys}, for example, is an absolute measure. On the other hand, the α required to achieve the same R_{sys} as that of some other system (e.g. TMR), is a comparative measure.

VARIATIONS IN SWITCH DESIGNS

H.simplex - We will call the hybrid scheme of Fig. 2 H.simplex if it uses a nonredundant switch. We have already established that if R_{sw} is assumed to be independant of m, the R_{sys} increases with m. With the linear model proposed earlier, the R_{sys} for H.simplex is given by

$$R_{H.simplex} = R^{m\alpha}.\{ 1 - m(1-R)^{m-1}R - (1-R)^m \} \quad (6)$$

The R_{sys} no longer increases uniformly. Fig. 5a and 5b show the varition of $R_{H.simplex}$ as a function of m for two values of the parameter α (0.1,0.01), and for various values of R. All of these exhibit a definite maxixmum. The optimum value, m_{max}, of the number of modules for maximum R_{sys}, is higher for lower R or lower α. Differentiaing the $R_{H.simplex}$ with respect to m, and equating the resultant expression to zero, we get the following equation :

$$\alpha \ln R = q^{m-1}.\{ R + (\alpha \ln R + \ln q).(mR + q) \} \qquad (8)$$

where $q = 1-R$.

This equation may be numerically solved for m_{max}. Values of m_{max} for H.simplex are plotted in Fig. 6.

It may be noted from these graphs, that m_{max} is about 4 to 6 for most practical cases. This means that only 1 to 3 spares should be used. In Fig. 6, m_{max} exceeds 6 only for $\alpha \leq 10^{-3}$. Recalling that α is the complexity of the switch component as compared to that of the module, more than 3 modules need be used only when the module is more than 1000 times as complex as the switch. For the iterative cell switch component which consists of 22 equivalent gates [SiewD73b], the module will be of the order of 22000 gates. A central processor of a computer has this complexity.

The MTI of the TMR over H.simplex scheme was found in the following manner. Assuming identical modules (having the same failure rate λ), a value for R_1, the reliability of a module in H.simplex was picked arbitrarily. The equation $R_{H.simplex}(R_1) = R_{TMR}(R_2)$ was solved for R_2. Since $R_1 = e^{-\lambda t}$ and $R_2 = e^{-\lambda t}$, $\ln R_2/\ln R_1$ yields the desired MTI. When MTI > 1, the TMR has longer t_m than H.simplex scheme. Results of this computation are presented in Fig. 7. It is once more evident that for $\alpha = 0.1$, the TMR has longer t_m than H.simplex. For smaller α, H.simplex has longer t_m for smaller values of R_1.

Checker-Redundant Scheme (CRS) - As mentioned earlier, the R_{sys} for CRS under the "linear" model for the switch is

$$R_{CRS} = R^{m\alpha}.\{ 1 - (1-R^{1+\beta})^m \} \qquad (7)$$

The factor β appears in the exponent of R as an additive factor to unity. Consequently, for β's much smaller than 1 (e.g. 0.001), their effect on R_{CRS} is

negligible.

An analysis similar to that for H.simplex was carried out for CRS. Figures 8, 9 and 10 show the graphs of R_{crs}, m_{max} and MTI of the TMR over CRS, respectively. For CRS, m_{max} is given by

$$m = [\ ln\ \{\propto ln\ R\ /\ (ln\ (1-x) + \propto ln\ R)\}\ ]\ /\ ln\ (1-x) \qquad (9)$$

where $x = R^{1+\rho}$.

Results for CRS, as seen from the Figures 8 to 10, are quite comparable to those for H.simplex.

H.tmr - It is clear from the results presented so far that R_{sw} plays an important role in the behavior of the overall system reliability. Let us now consider a hybrid scheme with the same TMR core as before, but with a fault-tolerant switch. Although there are many ways in which the switch may be made more reliable, the simplest to analyze are those of relication. In particular, the "cell" in the iterative cell array design [SiewD73b] may be triplicated and voters may be used on the intercell signals.

Fig. 11a shows a typical pair of adjascent cells in the iterative cell array. Although only one intercell signal is shown for the sake of clarity, identical extensions to more intercell signals may be used. Fig. 11b shows a case, where a single voter is used between the two sets of triplicated cells. In this case, the improvement achieved may be only marginal, because although every cell stage is now more reliable, its reliability is multiplied by that of the voter. Further improvement is achieved by triplication of voters as indicated in Fig. 11c. We will refer to the scheme with a single voter between the cell stages (Fig. 11b) as H.tmr.sv, and the scheme with triplicated voters between the cell stages (Fig. 11c) as H.tmr.tv.

To model H.tmr.sv, consider the box drawn with a dotted line in Fig. 11b. Using what is generally is known as serial modelling [AbraJ73], every such box in the iterative array has to function properly for the switch to be functional. If R_{vc} is the reliability of the voter between the cells and R_c the cell reliability, then the reliability of the box is $R_{vc} . \{ 3R_c^2 - 2R_c^3 \}$. This is arrived at by using the fact that only two of the three cells need to be functional for the box to function properly. There are m such boxes, except that the first box is without the voter. R_{SWSV}, the R_{SW} for H.tmr.V, is therefore,

$$R_{SWSV} = Y . (R_{vc} . Y)^{m-1} \qquad (10)$$

where $Y = 3 R_c^2 - 2 R_c^3$

Hence, the R_{SYS} for the H.tmr.sv scheme is

$$R_{H.tmr.sv} = R_{SWSV} . \{ 1 - m(1-R)^{m-1} - (1-R)^m \} \qquad (11)$$

Since, in Fig. 11b, every cell was referred to only as a functional box, one may include in R_c, the associated control circuitry of a few gates as well so that the functional box represents the switch component. We may then model $R_c = R^{\alpha}$ as before. Similarly, the voter reliability is modelled as $R_{vc} = R^{v\alpha}$, where v is the complexity of the voter as compared to the cell and its associated circuitry. For the iterative cell array design in [SiewD73b], v was estimated to range between 0.2 and 0.3. Figures 12 to 14 represent the behavior of R_{SYS}, m_{max} and the MTI of the TMR over the scheme for H.tmr.sv. As predicted, the improvement over the H.simplex scheme is only slight.

To model H.tmr.tv, consider the boxes drawn with the dotted lines in Fig. 11c. Now, for every stage to be functional, at least two of the three boxes have to functional properly. Every box has the reliability of $R_{vc}.R_c$, and

hence, the reliability of a stage is $\{ 3 R_{vc}^2.R_c^2 - 2 R_{vc}^3.R_c^3 \}$. Again there are (m-1) stages with the voters, and one without them. R_{SW3V}, the R_{SW} for H.tmr.tv scheme, is therefore,

$$R_{SW3V} = Y \cdot \{ 3 R_{vc}^2.R_c^2 - 2 R_{vc}^3.R_c^3 \}^{m-1} \qquad (12)$$

where $Y = 3 R_c^2 - 2 R_c^3$

and the R_{SYS} for the H.tmr.tv scheme is

$$R_{H.tmr.tv} = R_{SW3V} \cdot \{ 1 - m(1-R)^{m-1} - (1-R)^m \} \qquad (13)$$

Again, we will model $R_c = R^{\alpha}$ and $R_{vc} = R^{v\alpha}$. With the treatment similar to that in previous cases, Figures 15 to 17 are obtained. The improvement of H.tmr.tv scheme over H.simplex is much more significant than that of H.tmr.sv.

H.hc - Based on the iterative cell design for the switch in [SiewD73b], R. Ogus [OgusR73] suggested a switch design in which the next state and the intercell signals together were to be encoded in the Hamming (8,4) code [PeteW72]. An actual design using the state tables from [OgusR73] indicated the encoded switch to be approximately seven times as complex as the iterative cell in [SiewD73b]. The design was carried out such that the Hamming code assumption of bit indepenence was not violated. With this design as the basis, the reliability of any particular signal (next state or intercell) was assumed to be $R^{7\alpha}$. Of the eight signals, the Hamming code can tolerate one erroneous signal. The R_{SW} for this scheme is

$$\{ (R^{7\alpha})^8 + 8 (R^{7\alpha})^7 (1-R^{7\alpha}) \}^m$$

The R_{SYS} for H.hc scheme is, therefore, given by

$$R_{H.hc} = \{ R^{56\alpha} + 8 R^{49\alpha} (1-R^{7\alpha}) \}^m \cdot \{ 1 - m(1-R)^{m-1} - (1-R)^m \} \qquad (14)$$

Figures 18 to 20 show the R_{SYS}, m_{max}, and the MTI of the TMR over the scheme for H.hc. Note the change of scale in Fig. 18 from the ones used for

other R_{sys} graphs. It is evident from these graphs that the increased complexity of the switch seriously affects the performance of the scheme.

II.rl - Finally, we consider the schemes that achieve fault-tolerance without voters. We refer to the schemes such as Quadded Logic [TryoJ56]. The fact that a stage may leave a fault uncorrected makes the reliability analysis of the quadded logic scheme extremely difficult. A scheme that achieves fault-tolerance in a manner similar to quadded logic, but requires only double the number of gates, was suggested by [KlasT69]. The scheme, known as Radial Logic, makes use of circuit properties to mask faults. A detailed development of the reliability model for Radial Logic appears in [KlasT69]. We will only use the results from this source.

We will consider the switch design made fault-tolerant by modifying the circuit for radial logic. According to the aforementioned report, R_u, the reliability of an unredundant gate, is

$$R_u \simeq 1 - 2\,Q_o - 2\,Q_s, \tag{15}$$

and R_r, the reliability of the corresponding redundant gate is

$$R_r \simeq 1 - 16\,Q_s^2 - 4\,Q_o^2 - 32\,Q_s\,Q_o - 2\,Q_{rs}, \tag{16}$$

where

Q_o = the probability of a transistor open fault,

Q_s = the probability of a transistor short fault,

and Q_{rs} = the probability of a resistor short fault.

As suggested in [KlasT69], making the assumptions $Q_o = Q_s = Q$ and Q_{rs} negligible as compared to Q, we have

$$\left.\begin{aligned} R_u &\simeq 1 - 4\,Q \\ \text{and}\quad R_r &\simeq 1 - 52\,Q^2. \end{aligned}\right\} \tag{17}$$

Eliminating Q from these equations we get the R_r in terms of R_u as

$$R_r = 1 - 3.25\,(1-R_u)^2 \qquad (18)$$

Again using the iterative cell design as a basis, we model $R_u = R^{\alpha/22}$. The switch reliability is therefore,

$$\{\, 1 - 3.25\,(1-R^{\alpha/22})^2 \,\}^{22m}$$

and the R_{sys} is

$$R_{H.rl} = \{\, 1 - 3.25\,(1-R^{\alpha/22})^2 \,\}^{22m} \cdot \{\, 1 - m(1-R)^{m-1} - (1-R)^m \,\} \qquad (19)$$

Figures 21 to 23 depict the behavior of the H.rl scheme. This scheme exhibits higher reliability and longer t_m than the others considered here. It must be mentioned, however, that in obtaining the expressions for R_u and R_r in [KlasT69], second order effects were neglected.

Figures 24 to 26 present composite graphs for the various schemes described here. $R = 0.9$ and $\alpha = 0.1$ were chosen arbitrarily for this comparison.

CONCLUSIONS

In this discussion, we have shown that the switch reliability is an important factor in the system reliability and behavior. The often used assumption of the switch reliability being independant of the number of modules in the system is not only unrealistic, but may lead to wrong conclusions. Based on a few actual designs, it was proposed that the switch complexity be assumed to grow linearly with the number of modules.

Significant changes in the behavior of the system reliability were witnessed under this model. It was found that there exists a definite value for the number of modules for which the system reliability reached a maximum.

Furthermore, this optimum value of the number of modules corresponded to only a few spares - typically 2 or 3 - for most practical systems. These results concur with those presented in [OgusR73].

The mission time improvement of TMR over the various schemes showed that in some cases, the simple TMR scheme had longer mission times than the hybrid schemes. It was also seen from the mission time improvement graphs that if the switch was much simpler than the basic module (i.e. the switch component reliability was much more closer to unity than the module reliability), the hybrid schemes exhibit better performance than TMR.

The comparison of various fault-tolerant switch designs showed the radial logic, under its assumptions, to yield best results. Among the schemes that used voters, the TMR cell array switch with triplicated voters seemed to exhibit better behavior than the rest. The Hamming encoded design was the worst, perhaps, because of the peculiarity of the design.

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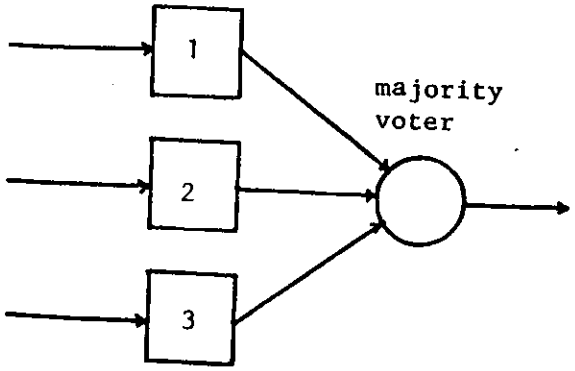


Figure 1(a). Triple-modular redundancy (TMR).

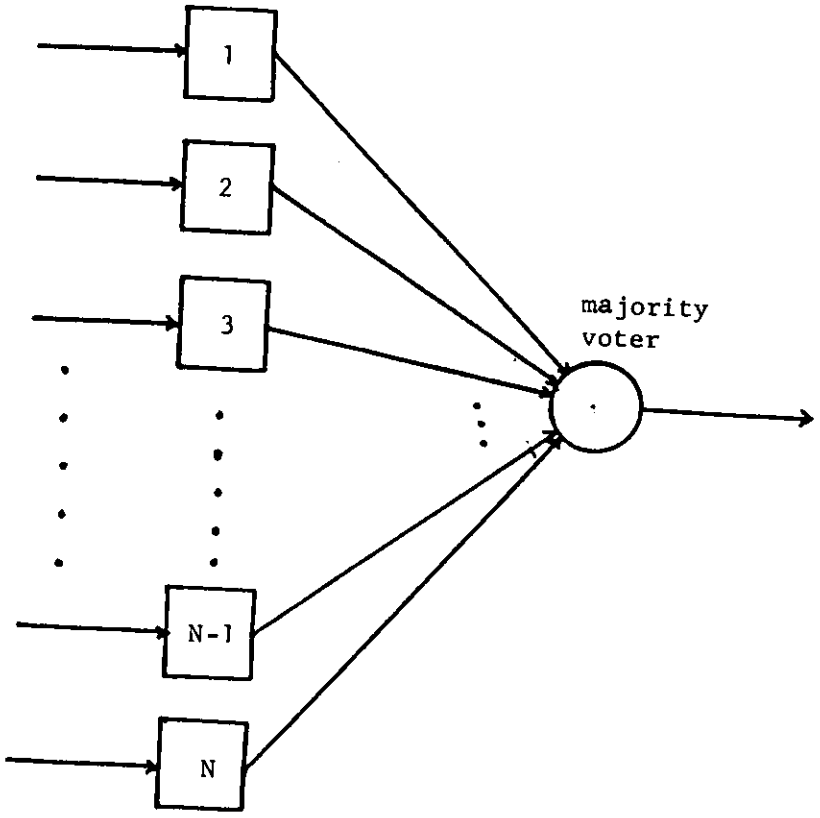


Figure 1(b). N-modular redundancy (NMR).

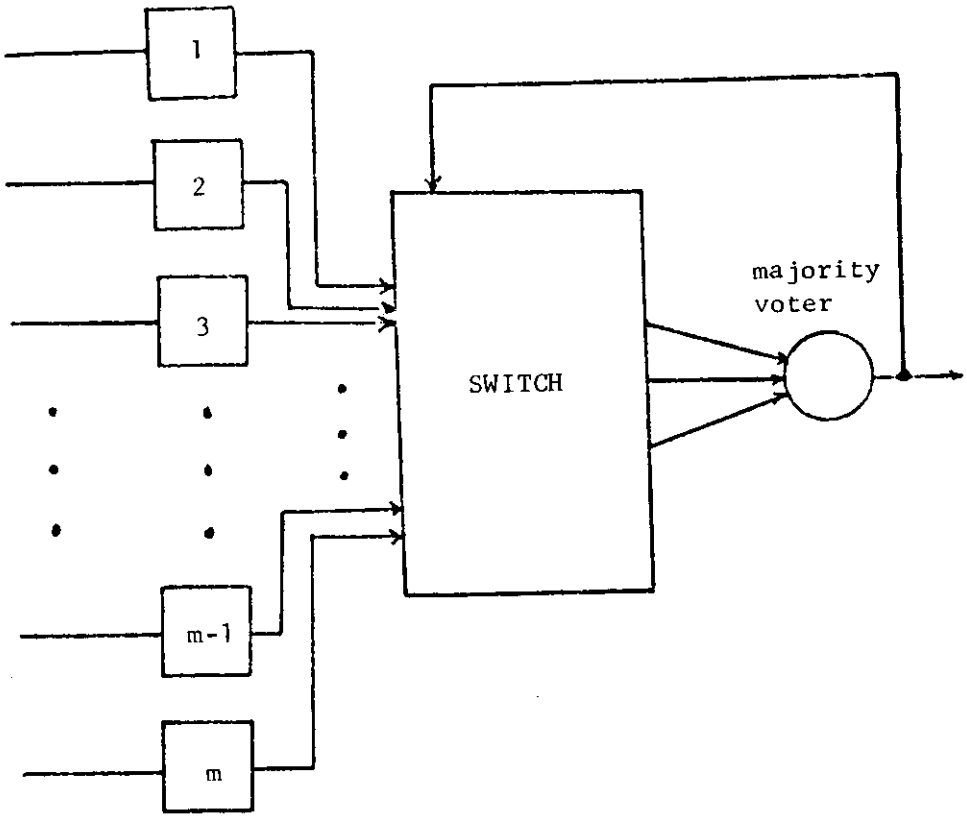


Figure 2. Hybrid redundancy scheme with a TMR core.

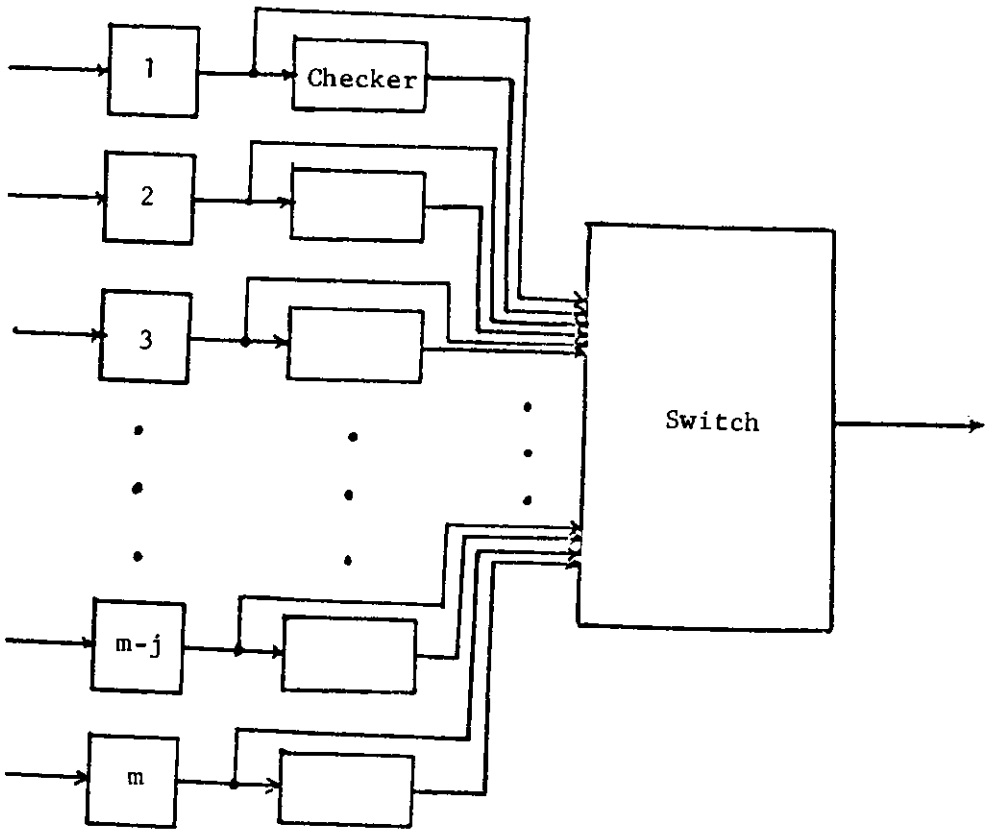


Figure 3. Checker-redundant scheme (CRS).

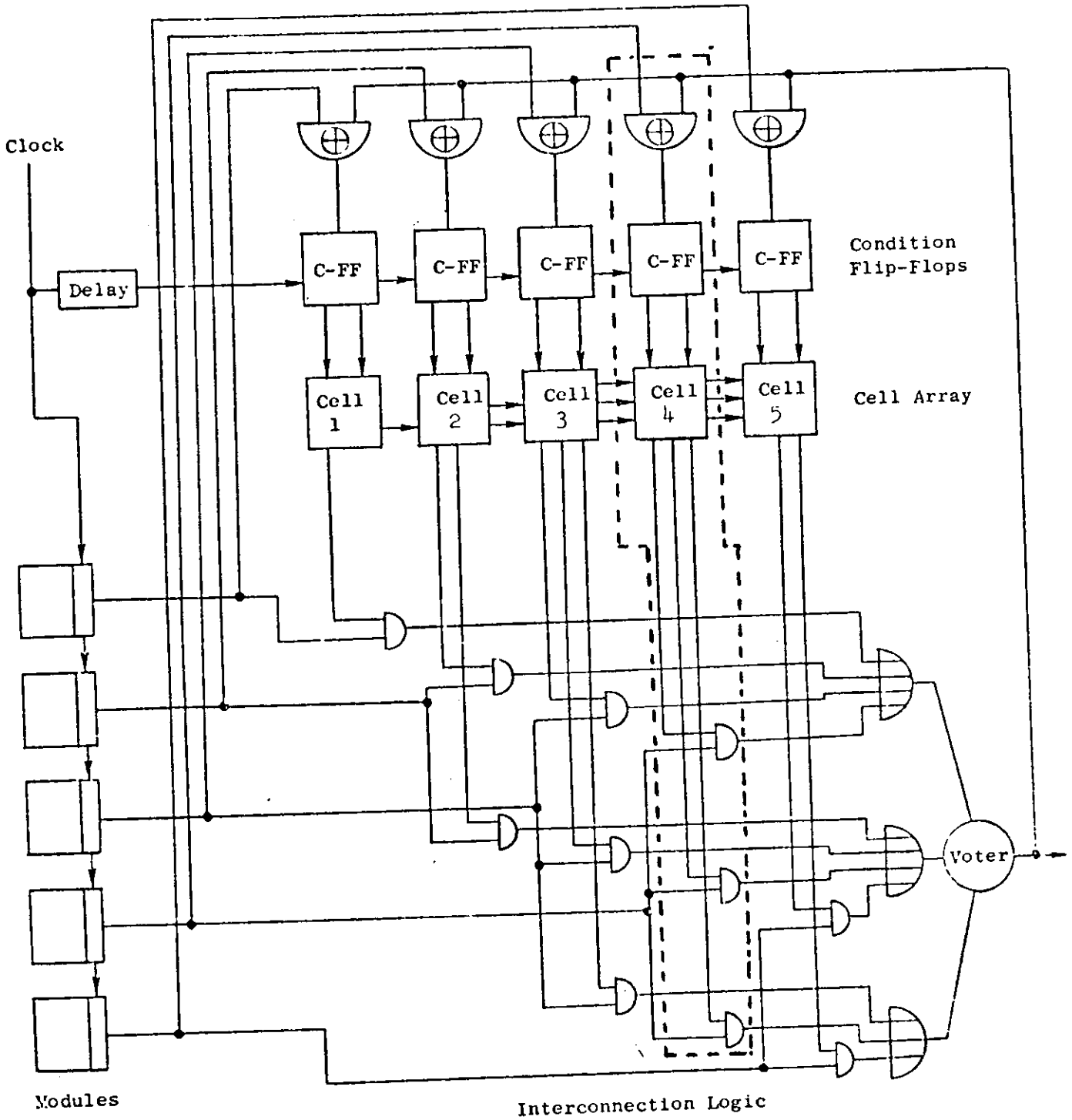


Fig. 4. An iterative cell switch for a TMR core and two standby spares

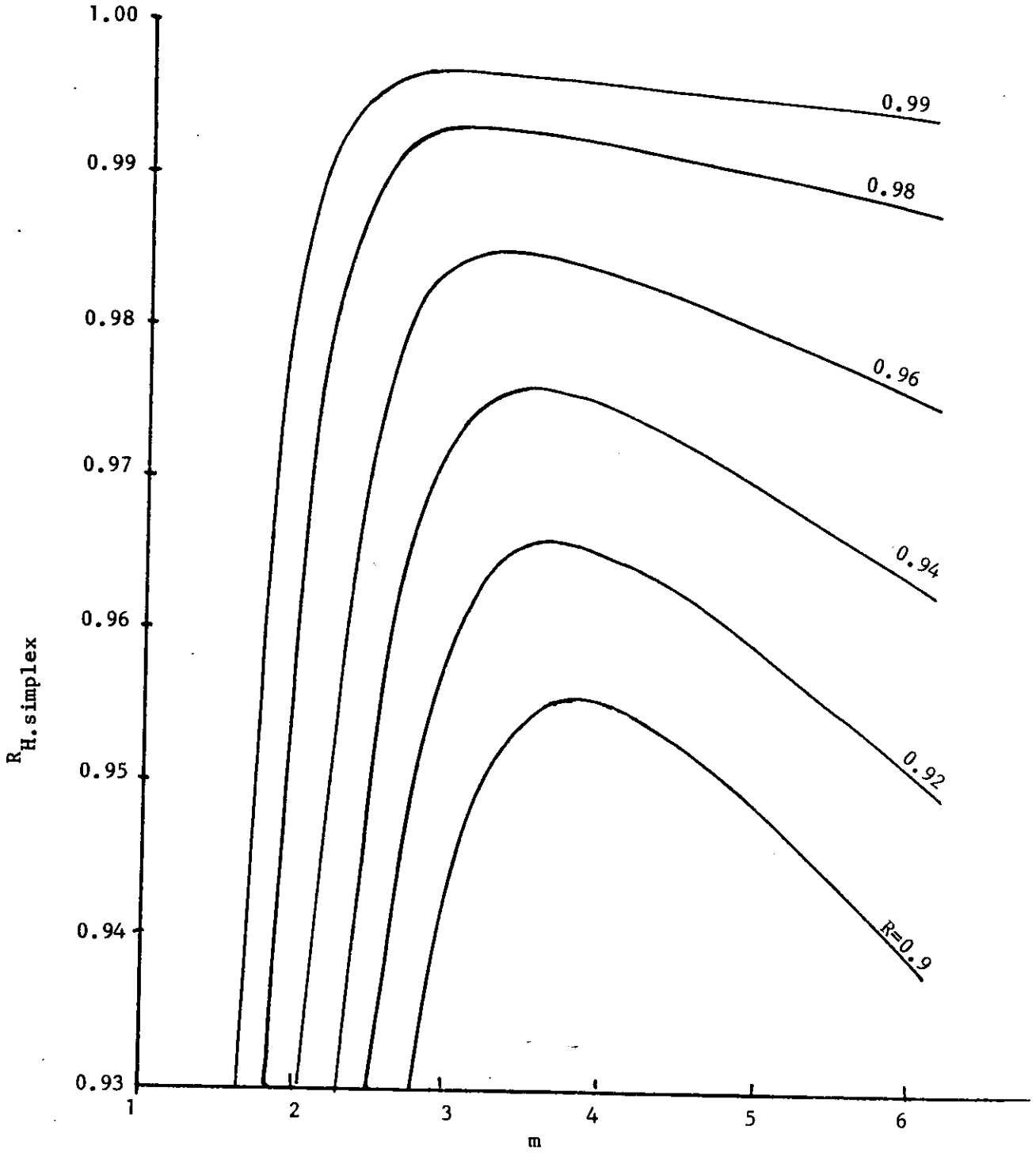


Figure 5(a). R_{sys} as a function of m for H.simplex, α=0.1.

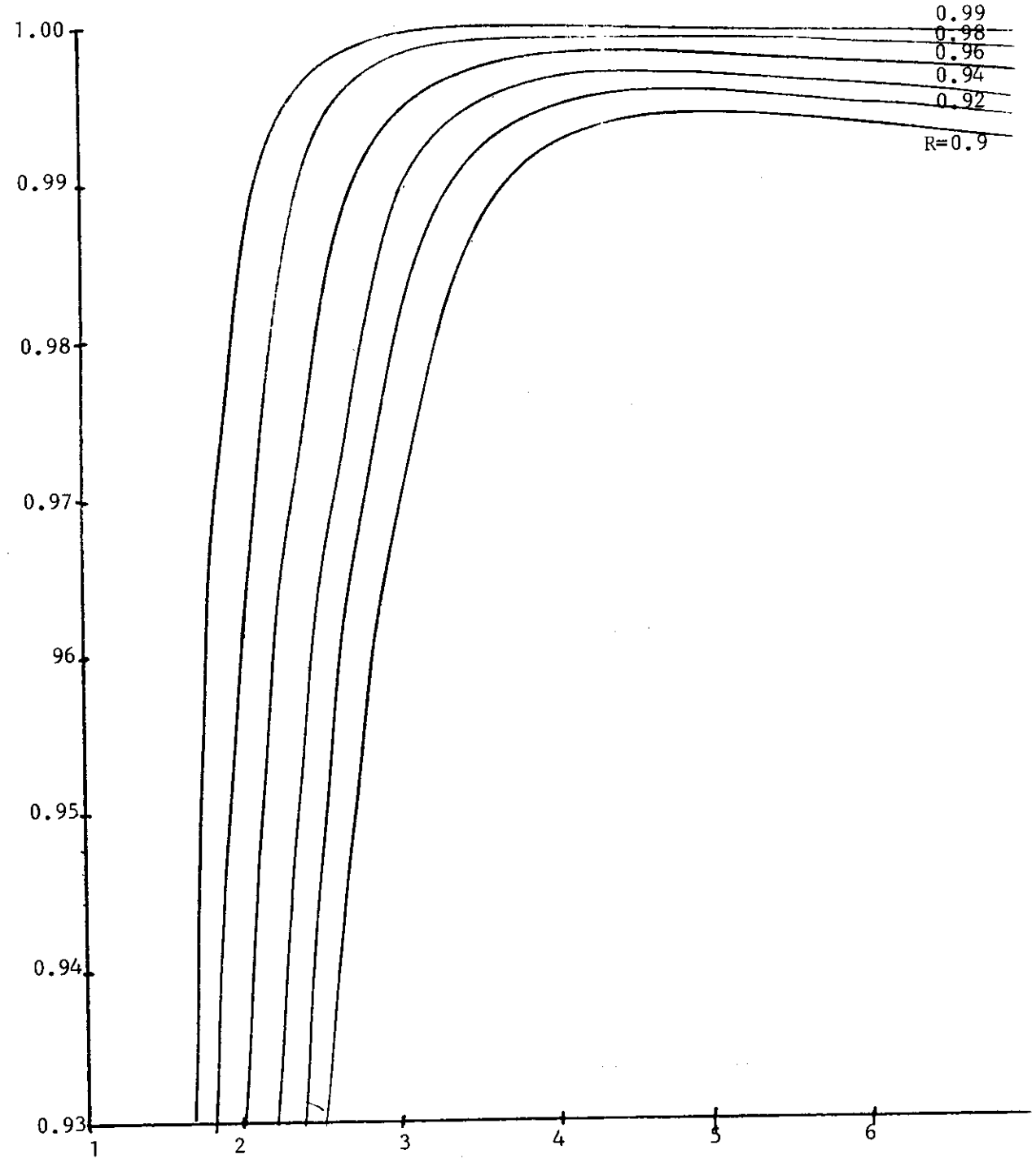


Figure 5(b). R_{sys} as a function of m for H.simplex, α=0.01.

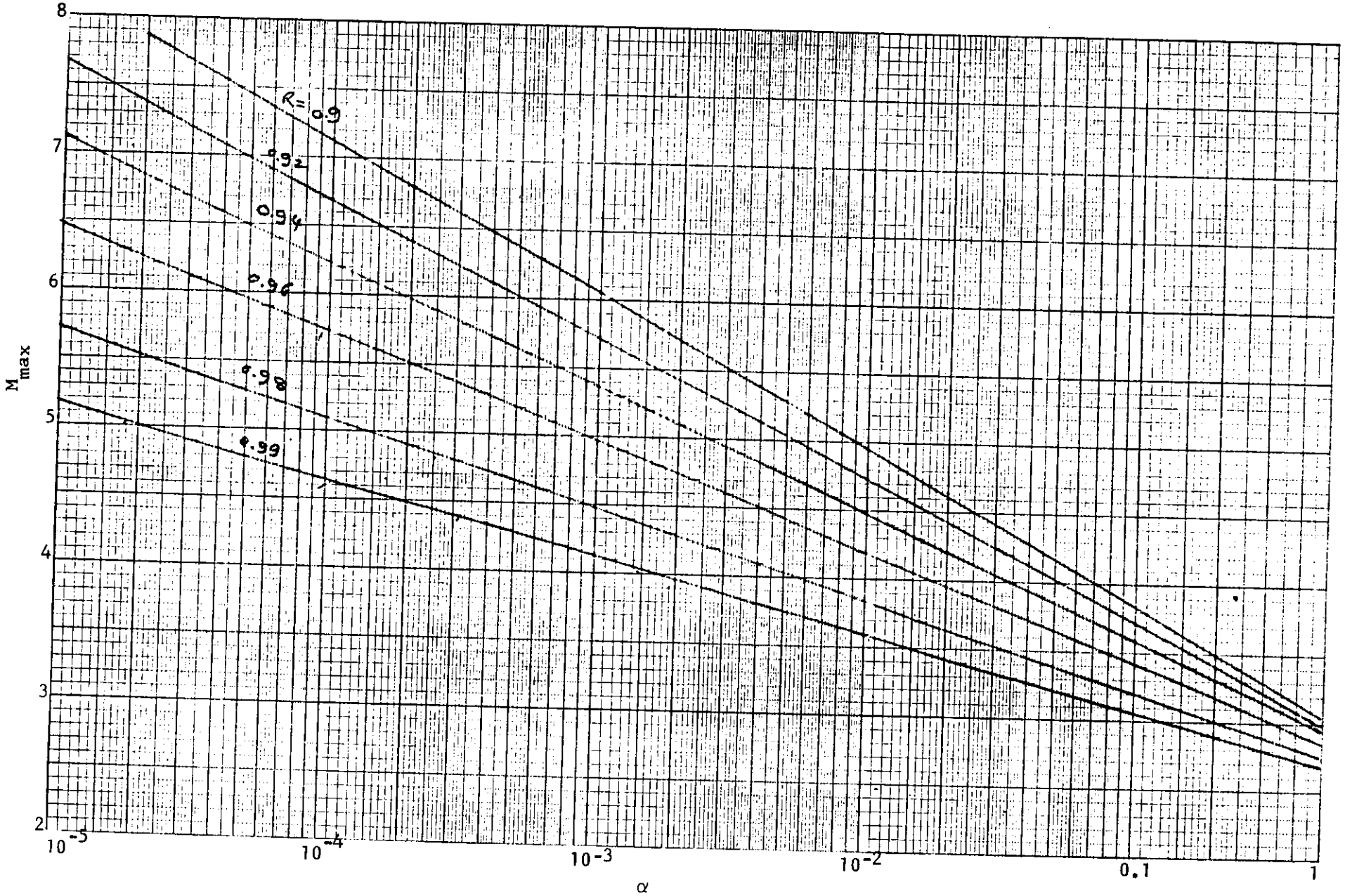


Figure 6. M_{max} as a function of α for H.simplex.

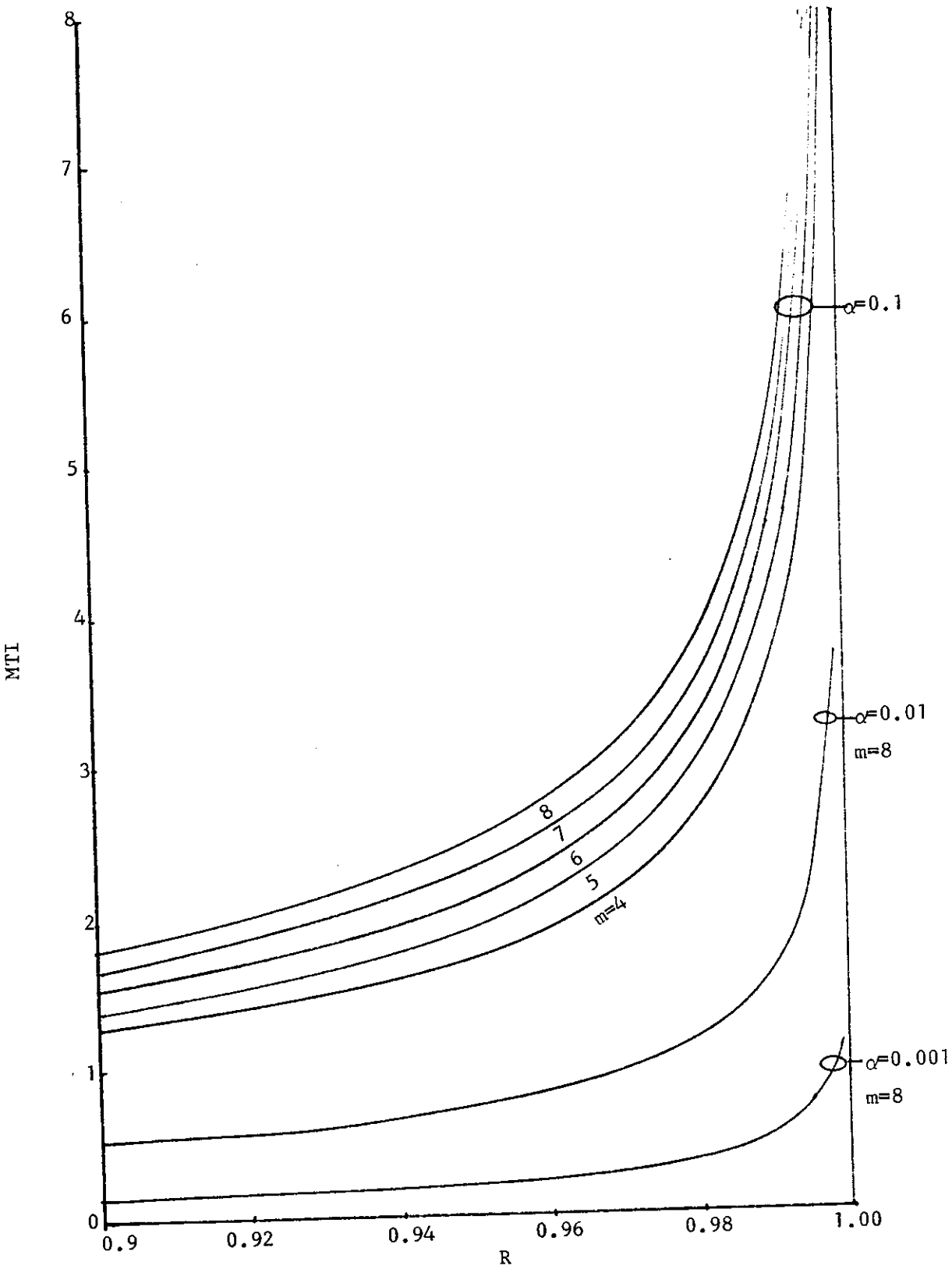


Figure 7. MTI of TMR over H.simplex.

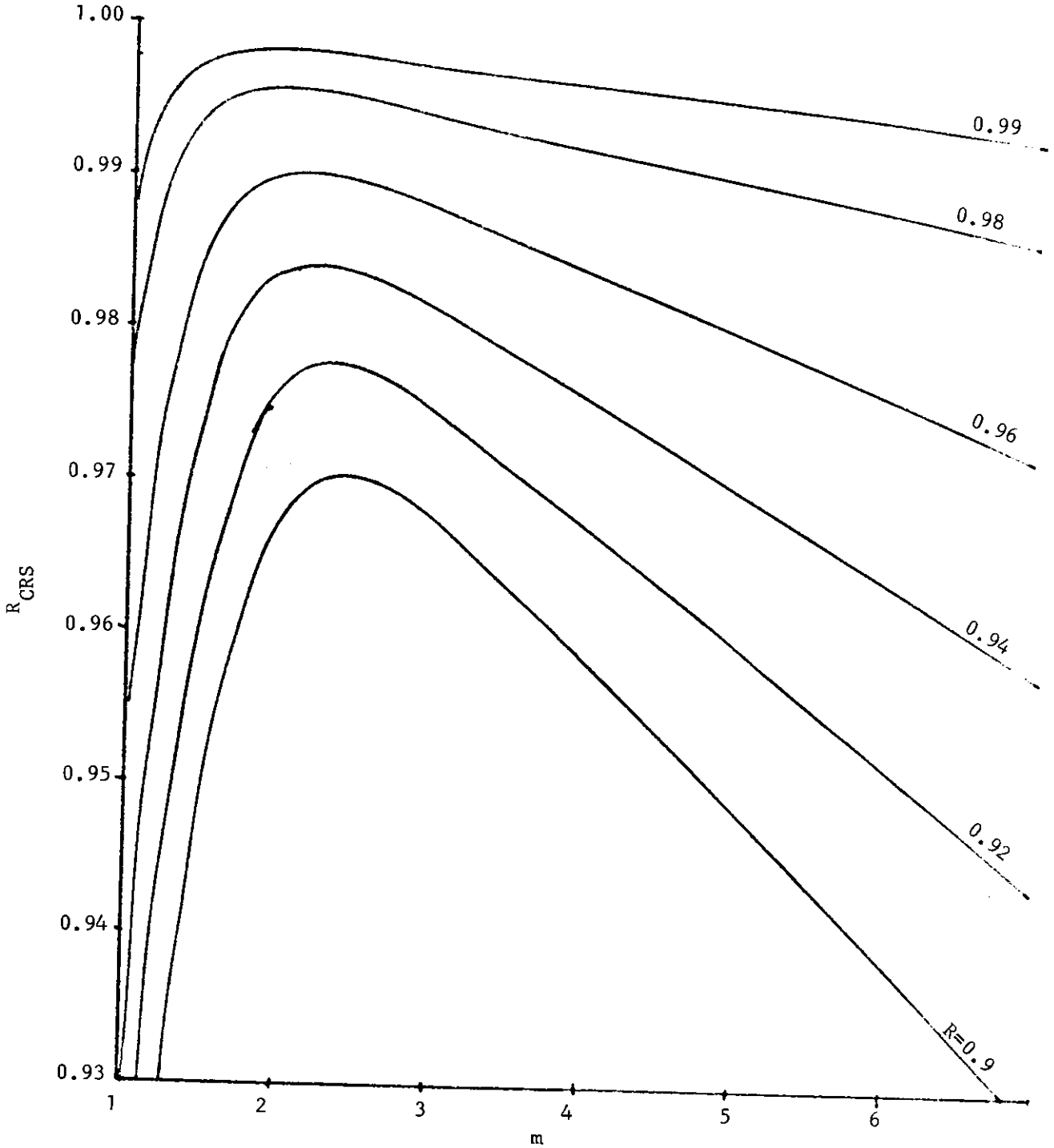


Figure 8. R_{sys} as a function of m for CRS, α=0.1, β=0.1.

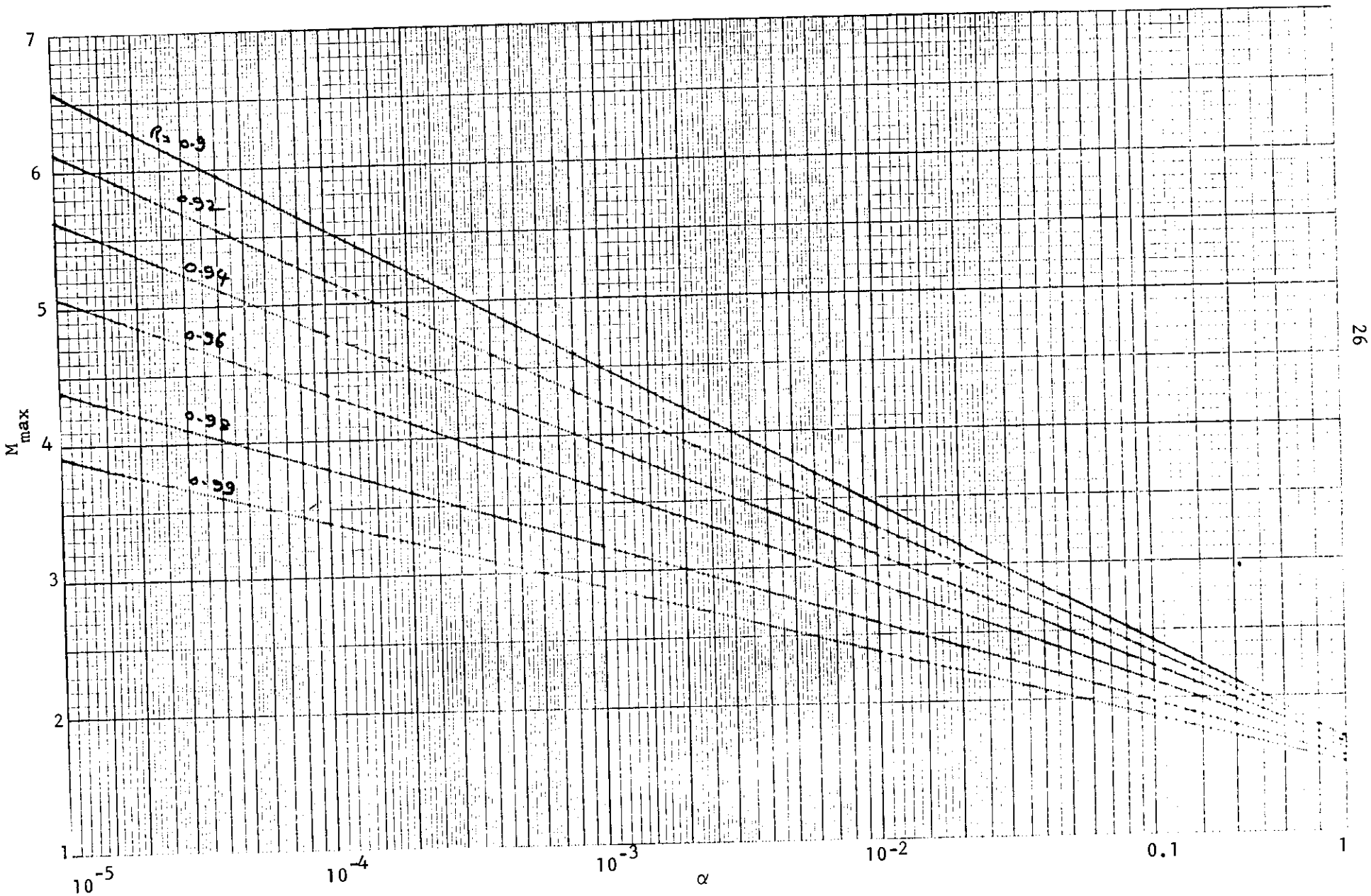


Figure 9. M_{max} as a function of α for CRS, β=0.1.

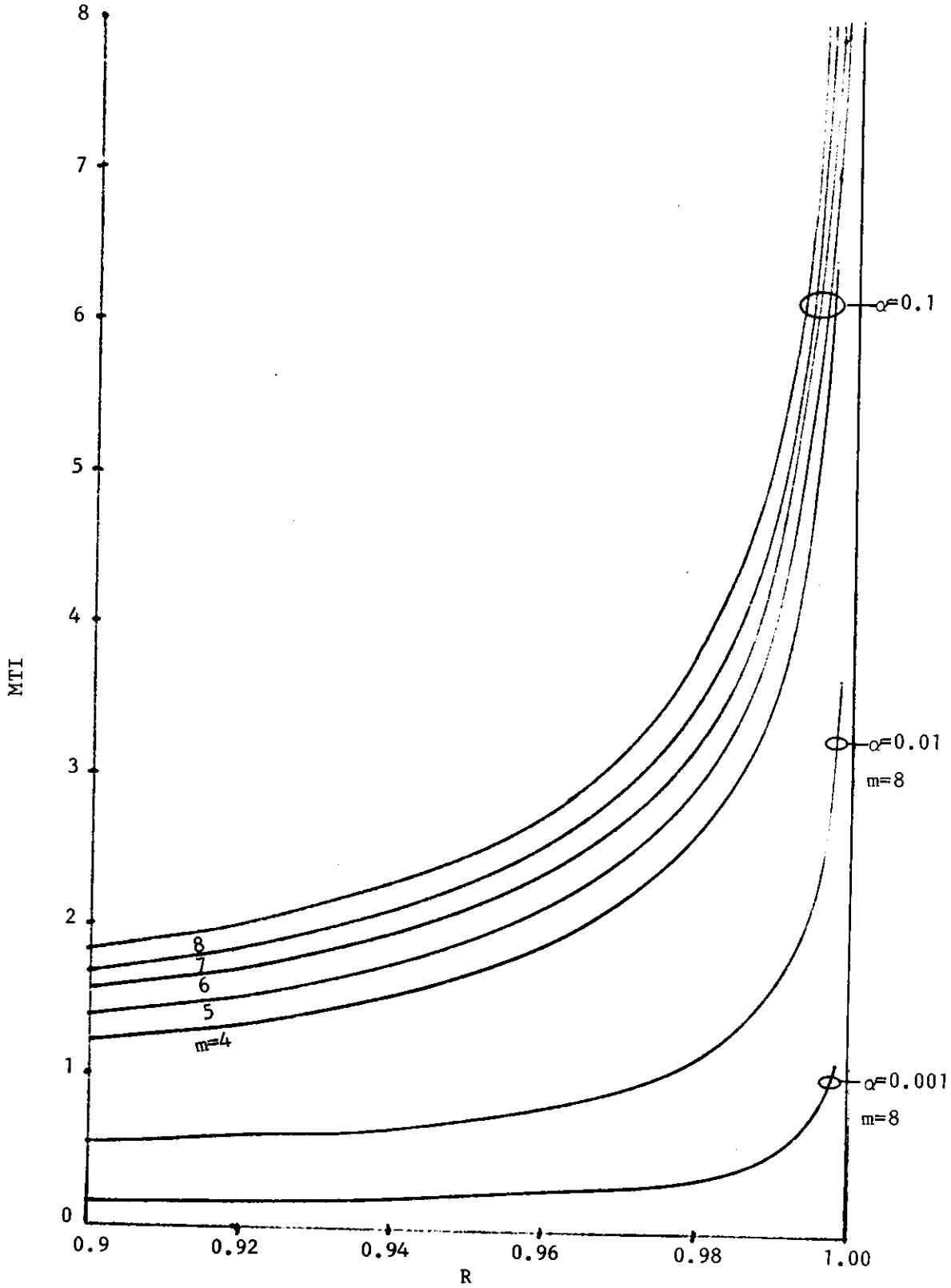
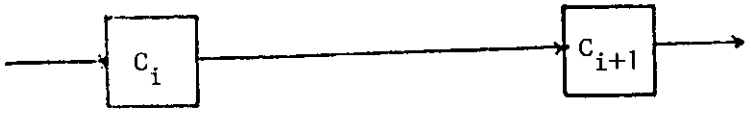
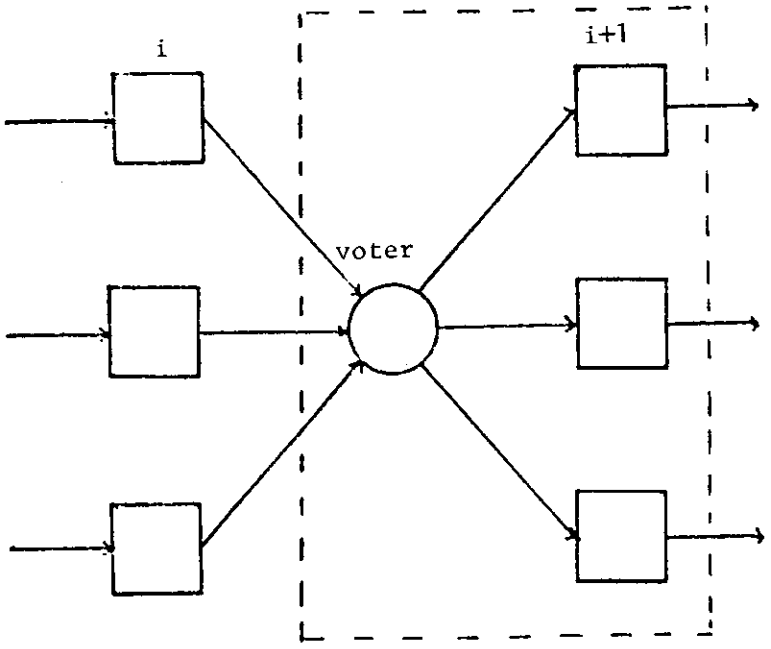


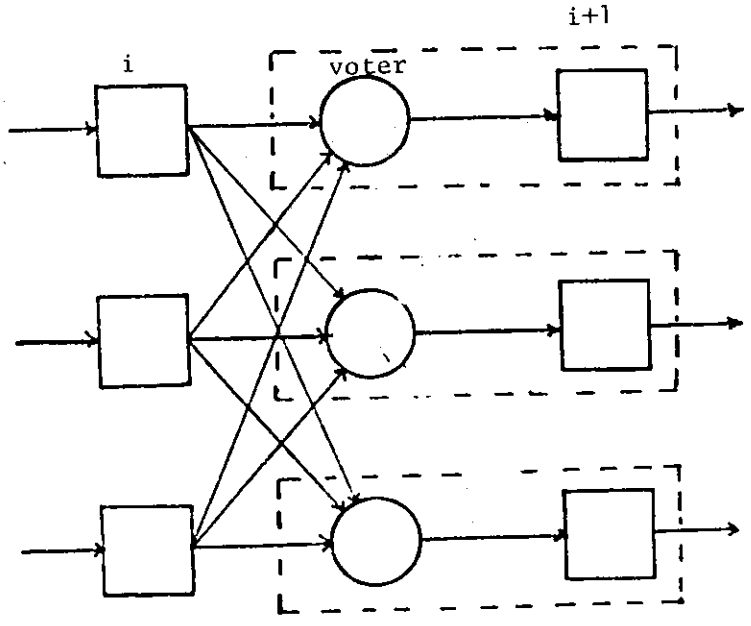
Figure 10. MTI of TMR over CRS, β=0.1.



(a) A typical pair of cells in the iterative array design.



(b) Triplicated cells with a single voter.



(c) Triplicated cells with triplicated voters.

Figure 11. Fault-tolerant switch design with triplicated cells (H.tmr).

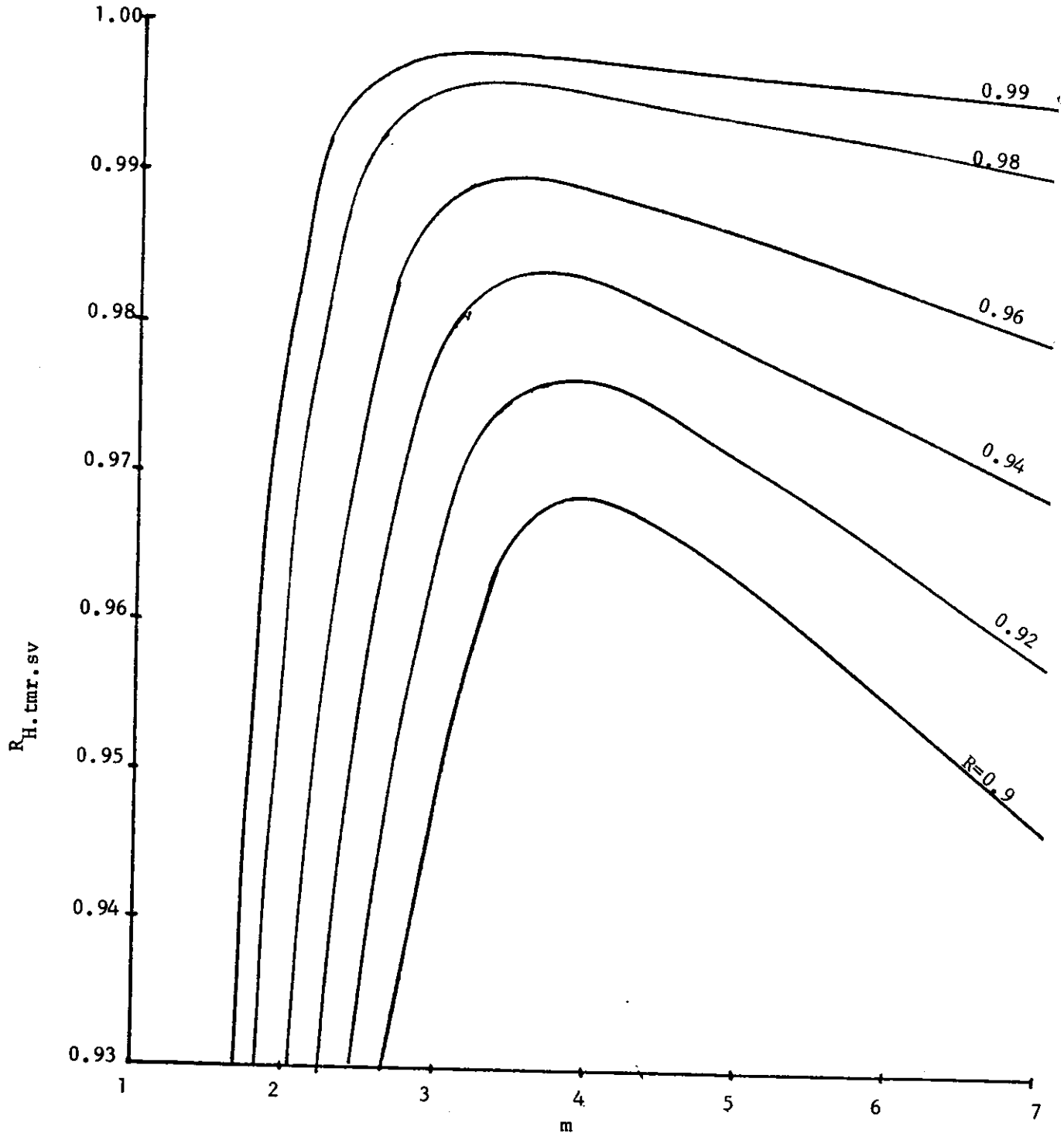


Figure 12. R_{sys} as a function of m for H.tmr.sv.

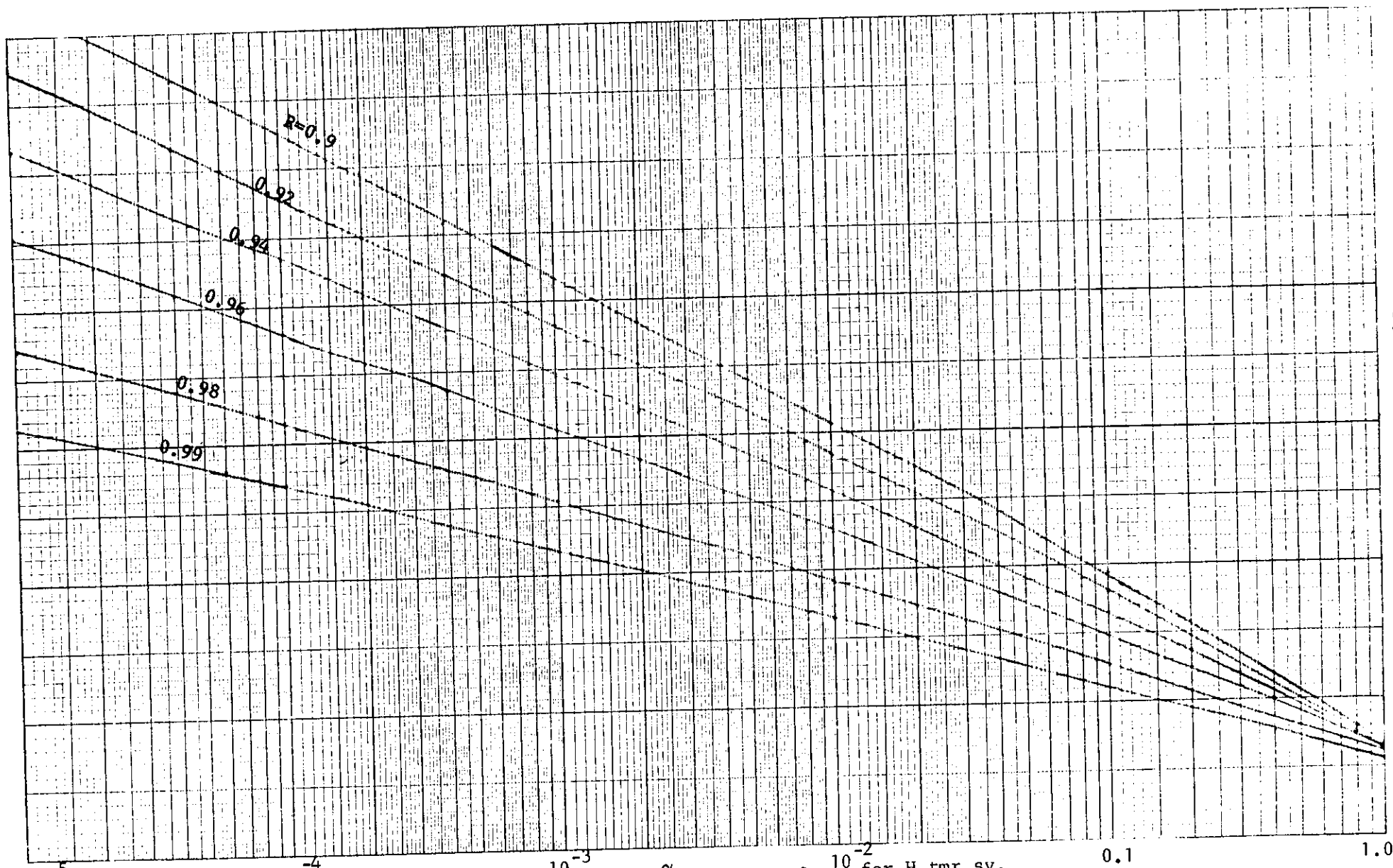


Figure 13. M_{max} as a α function of α for H.tmr.sv.

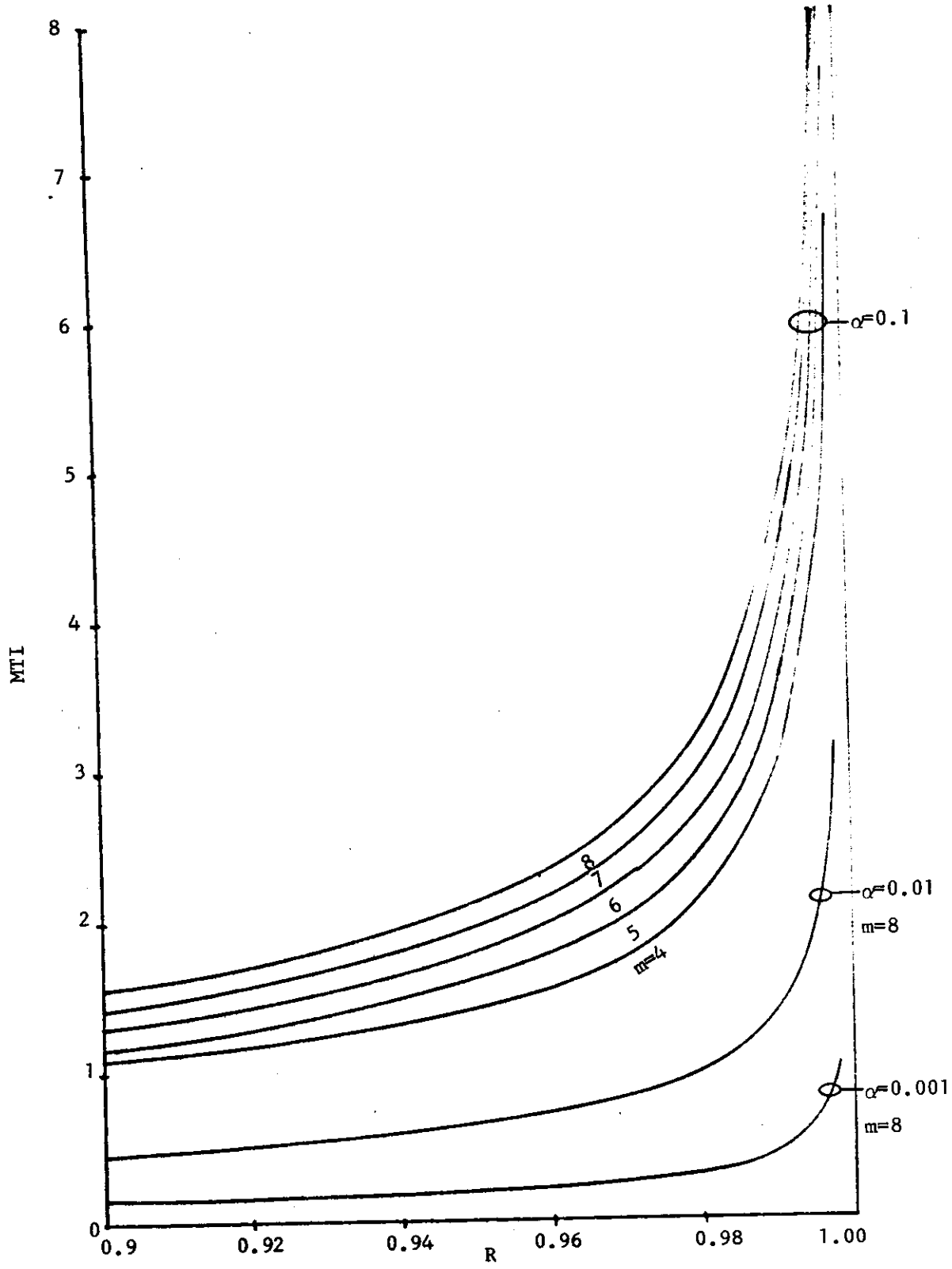


Figure 14. MTI of TMR over H.tmr.sv, ν=0.2

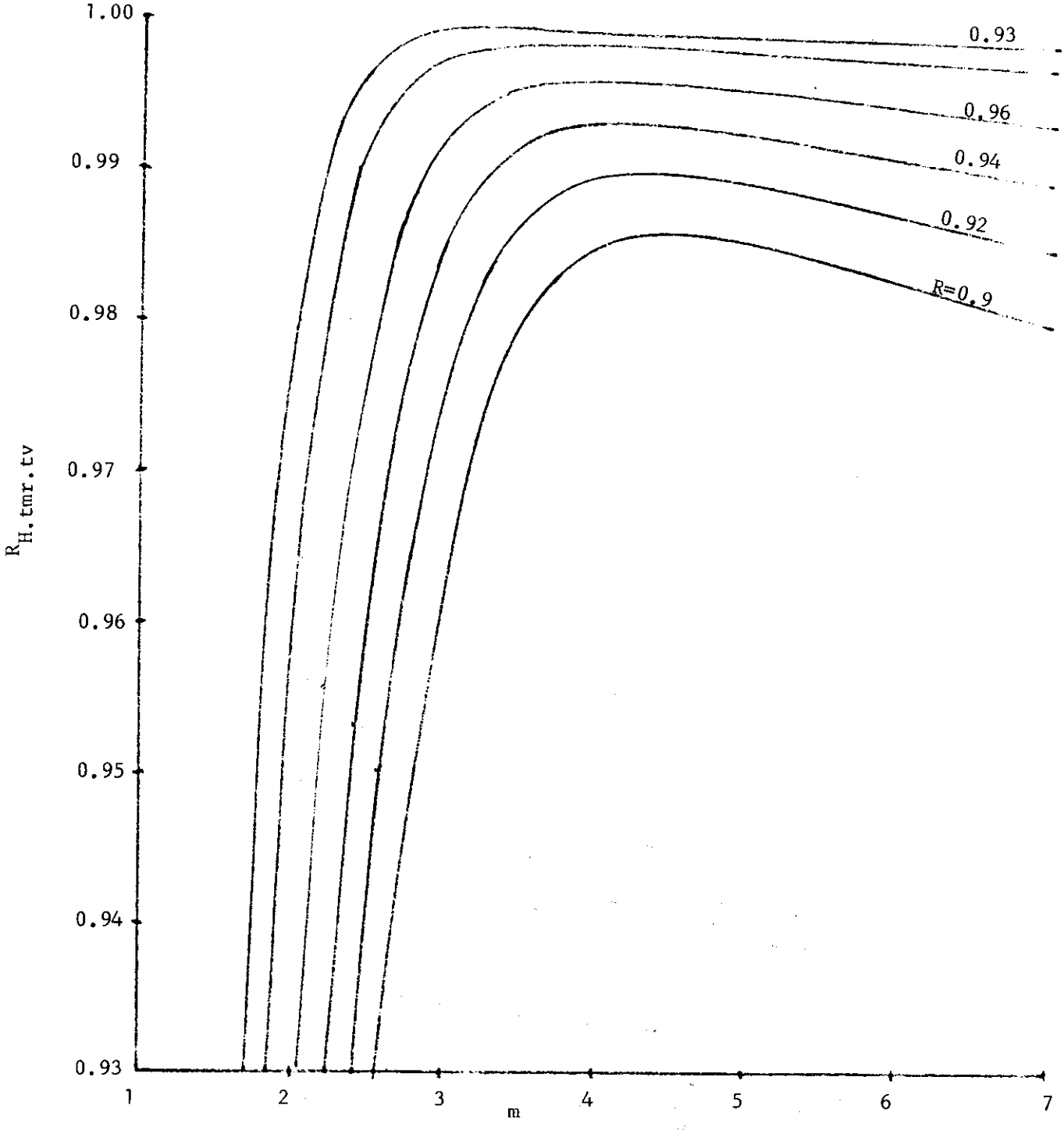


Figure 15. R_{sys} as a function of m for H.tmr.tv.

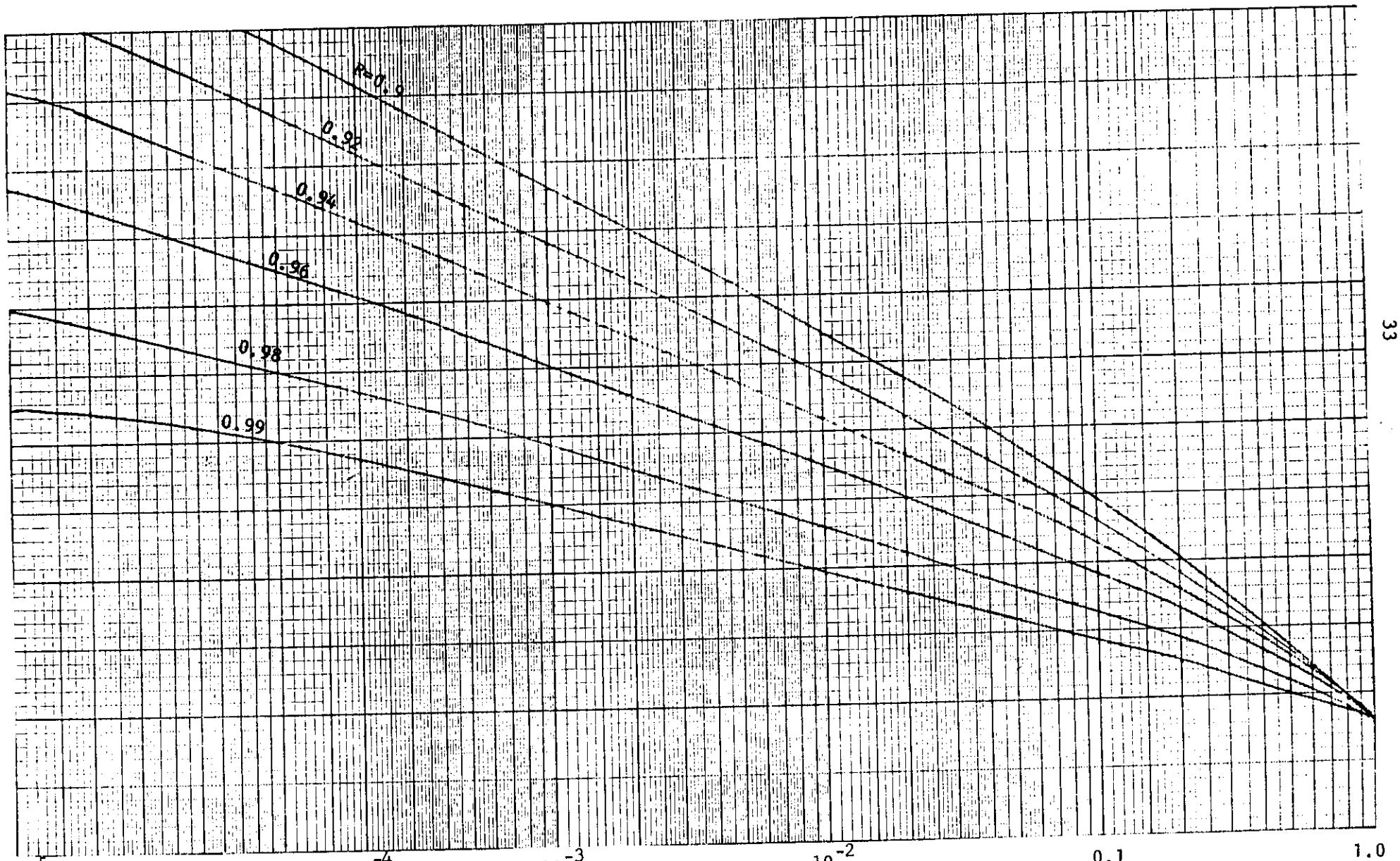


Figure 16. M_{max} as a function of α for H.tmr.tv.

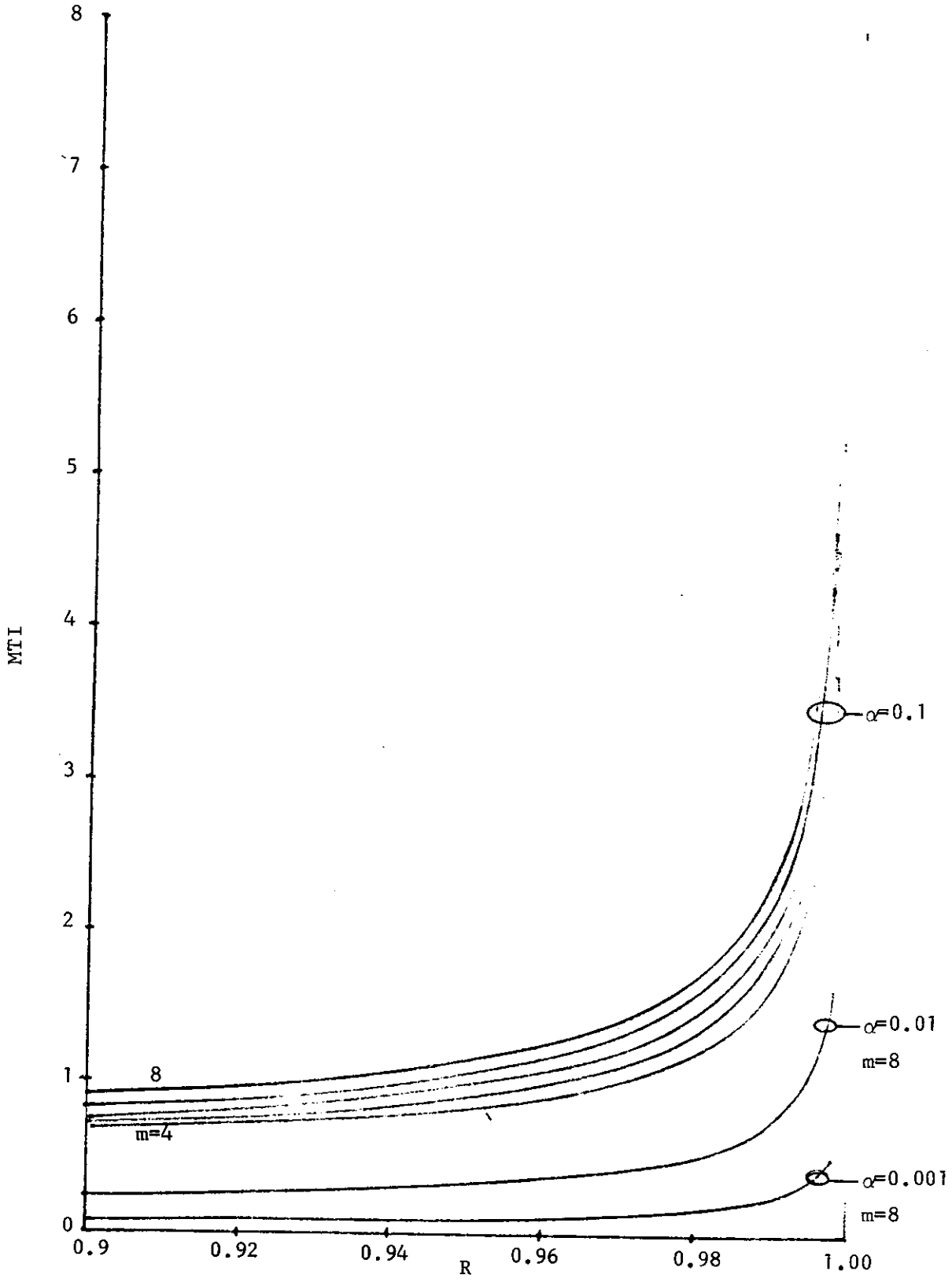


Figure 17. MIT of TMR over H.tmr.tv, ν=0.2.

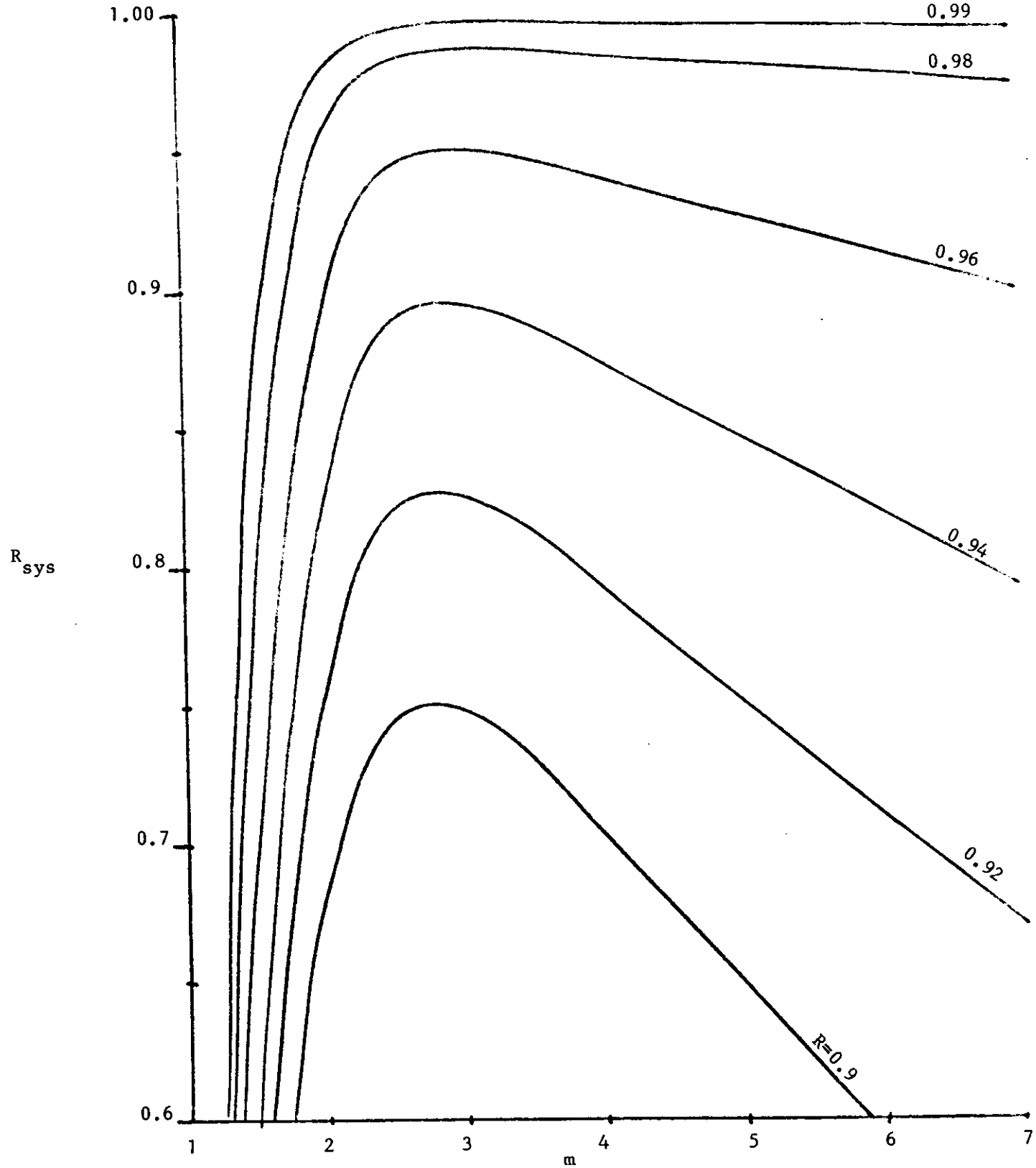


Figure 18. R_{sys} as a function of m for H.hc.

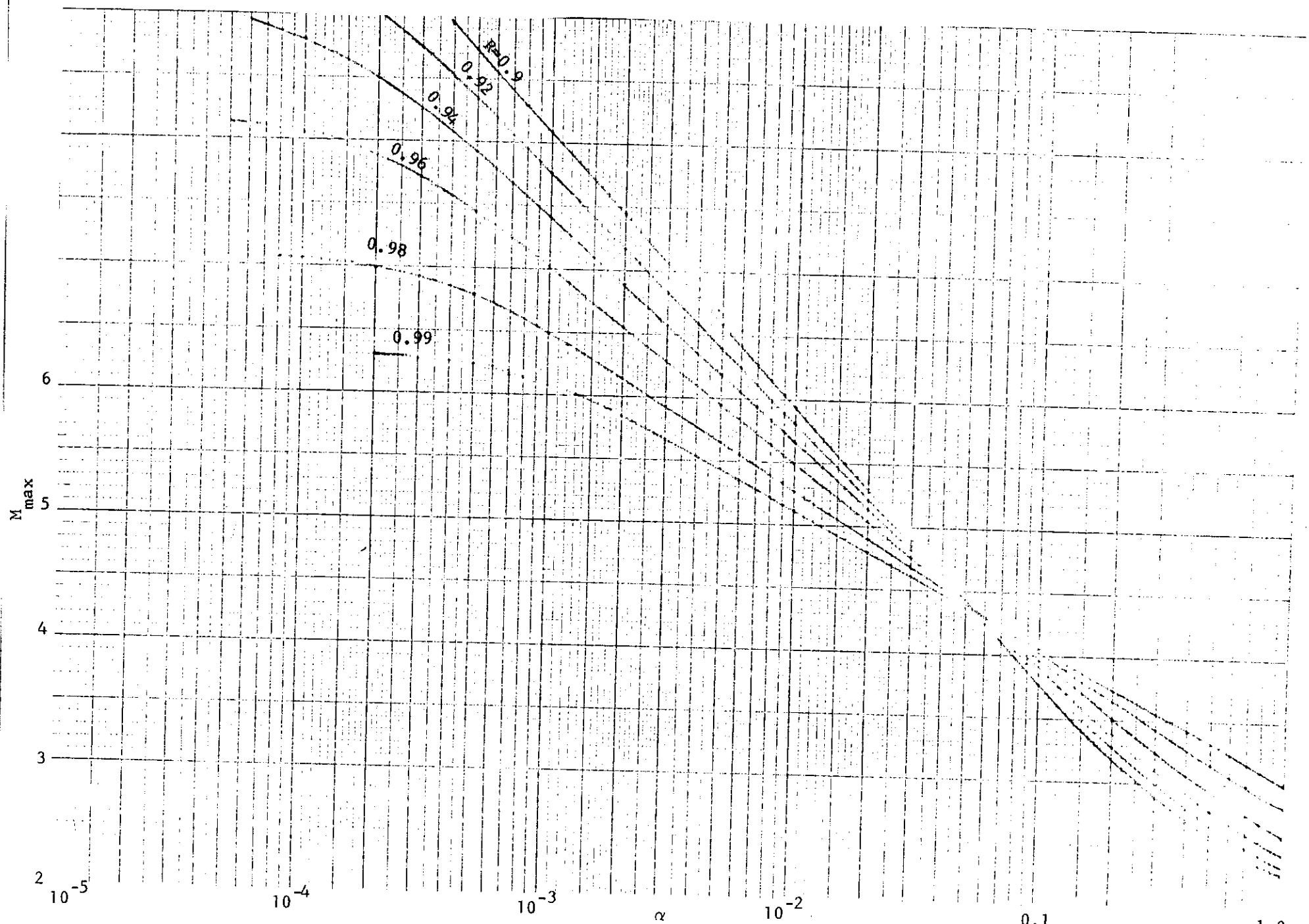


Figure 19. M_{max} as a function of α for H.hc.

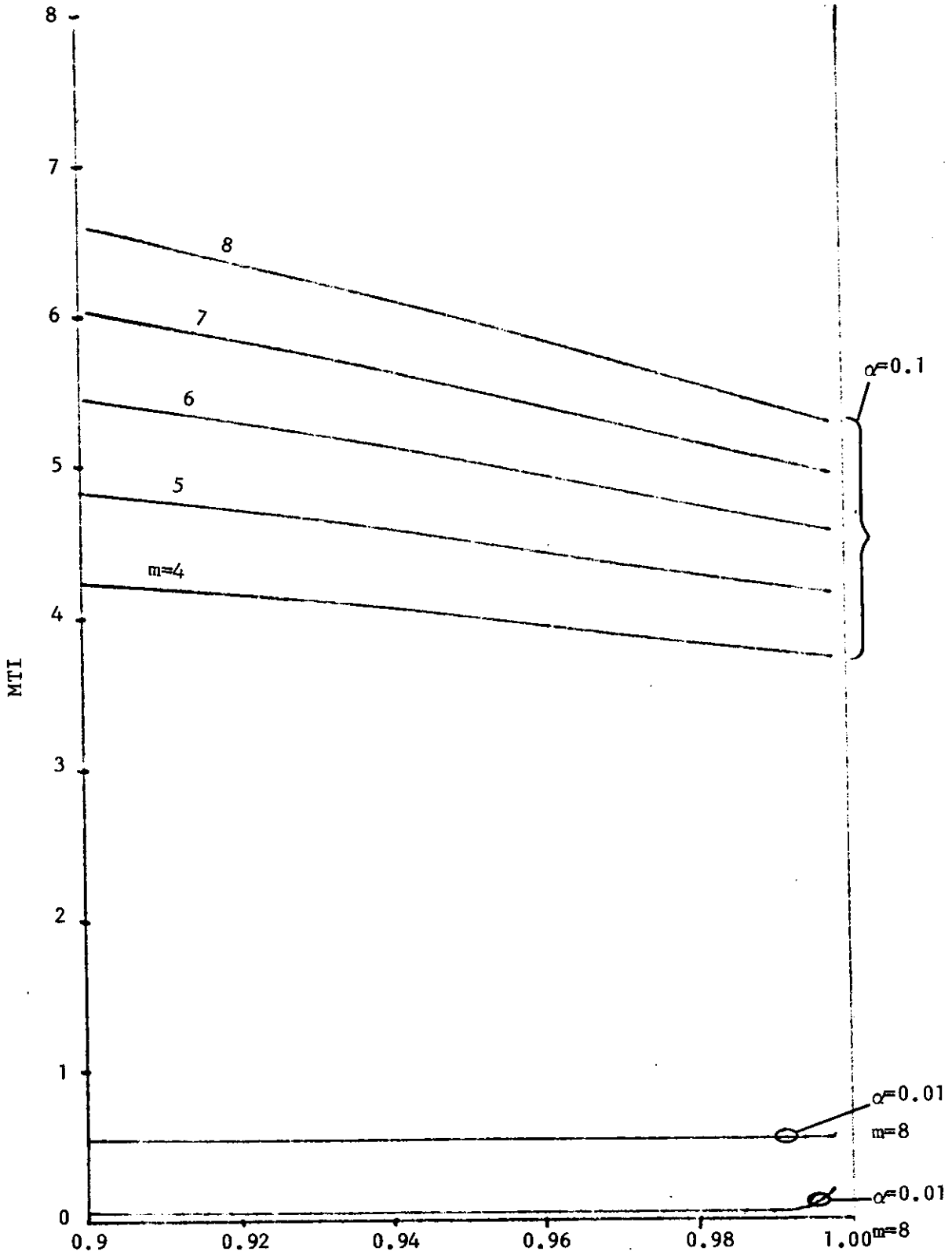


Figure 20. MTI of TMR over H.hc.

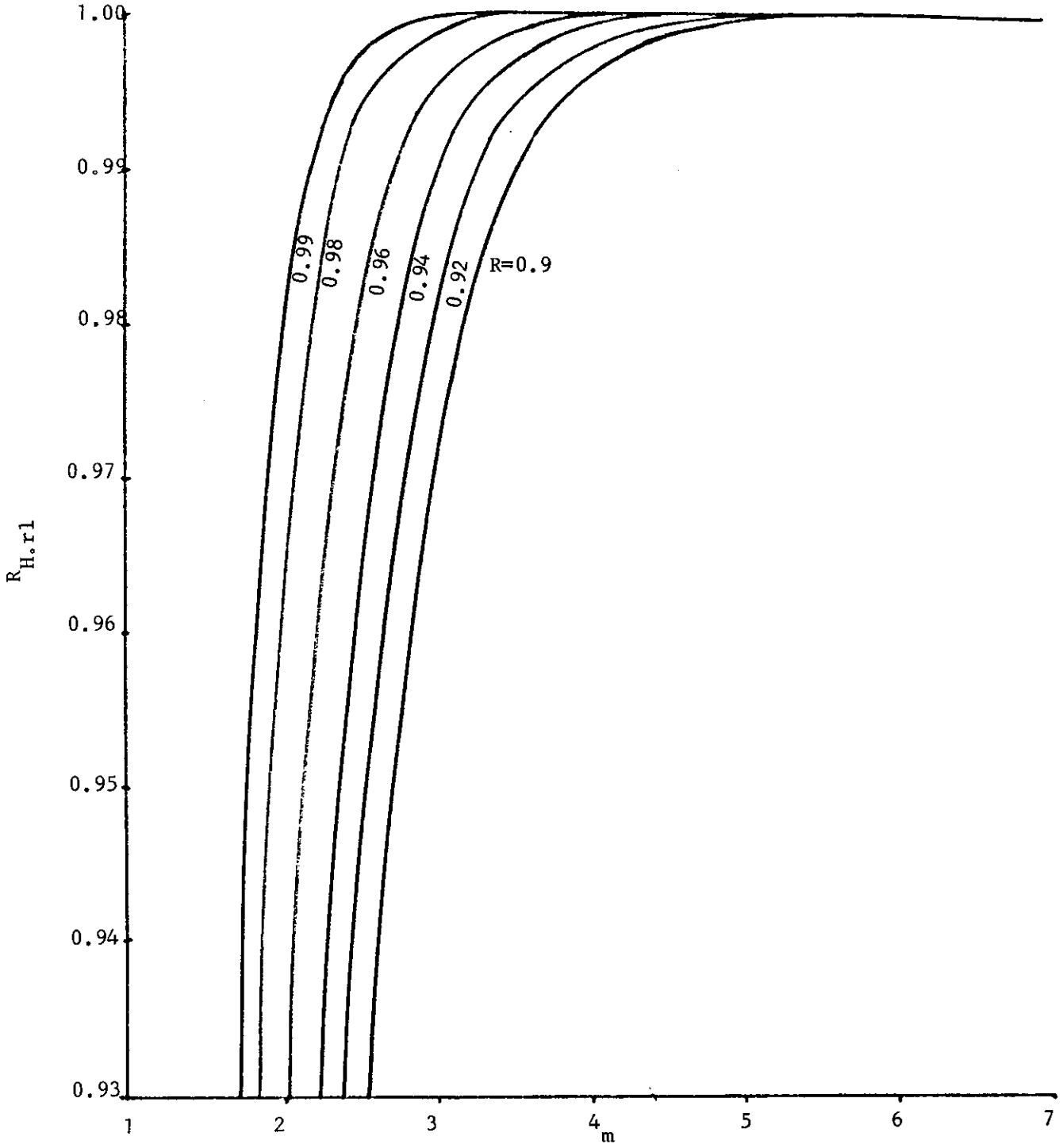


Figure 21. R_{sys} as a function of m for H.rl.

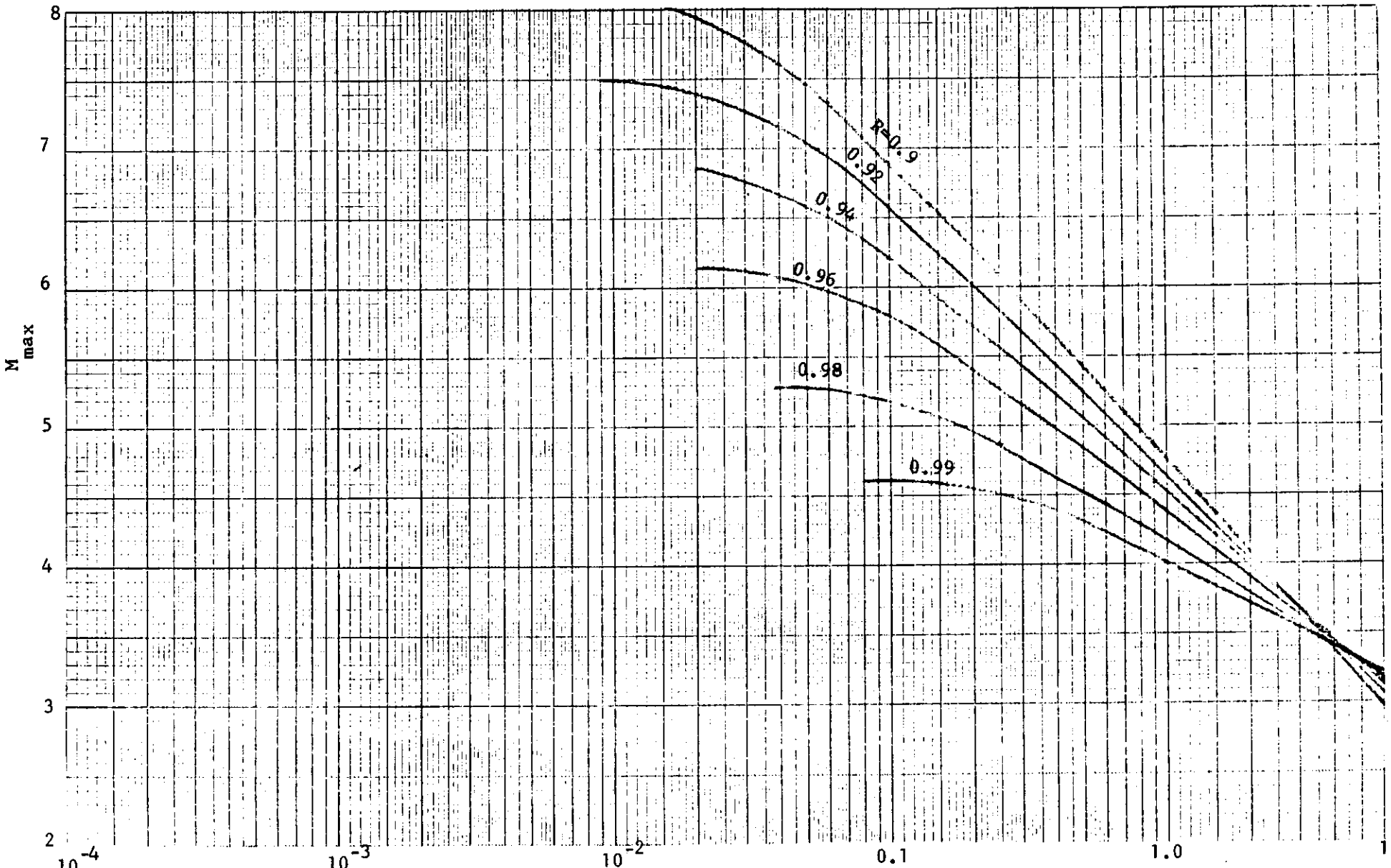


Figure 22. M_{max} as a function of α for H.rl.

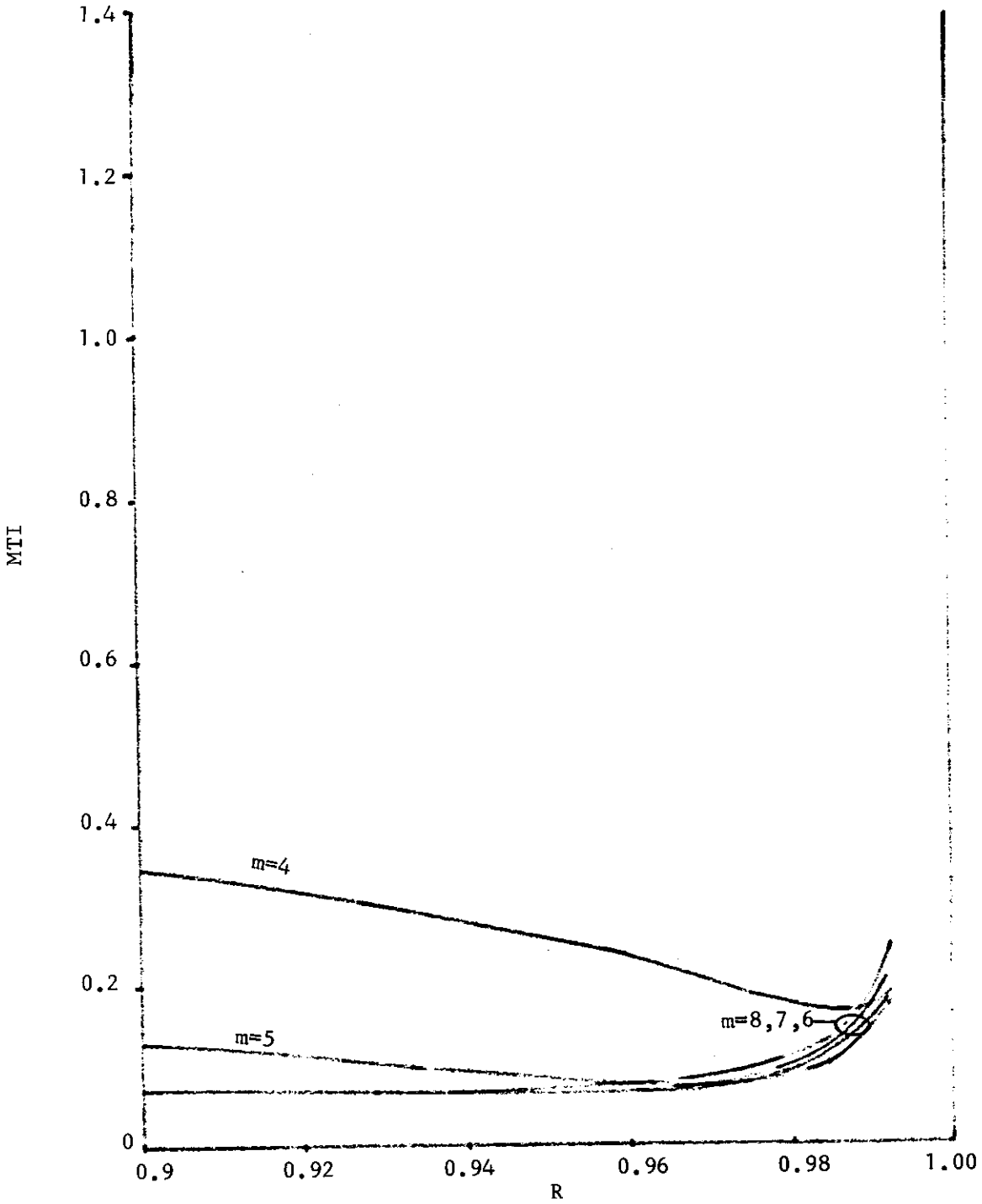


Figure 23. MTI of TMR over H.rl.

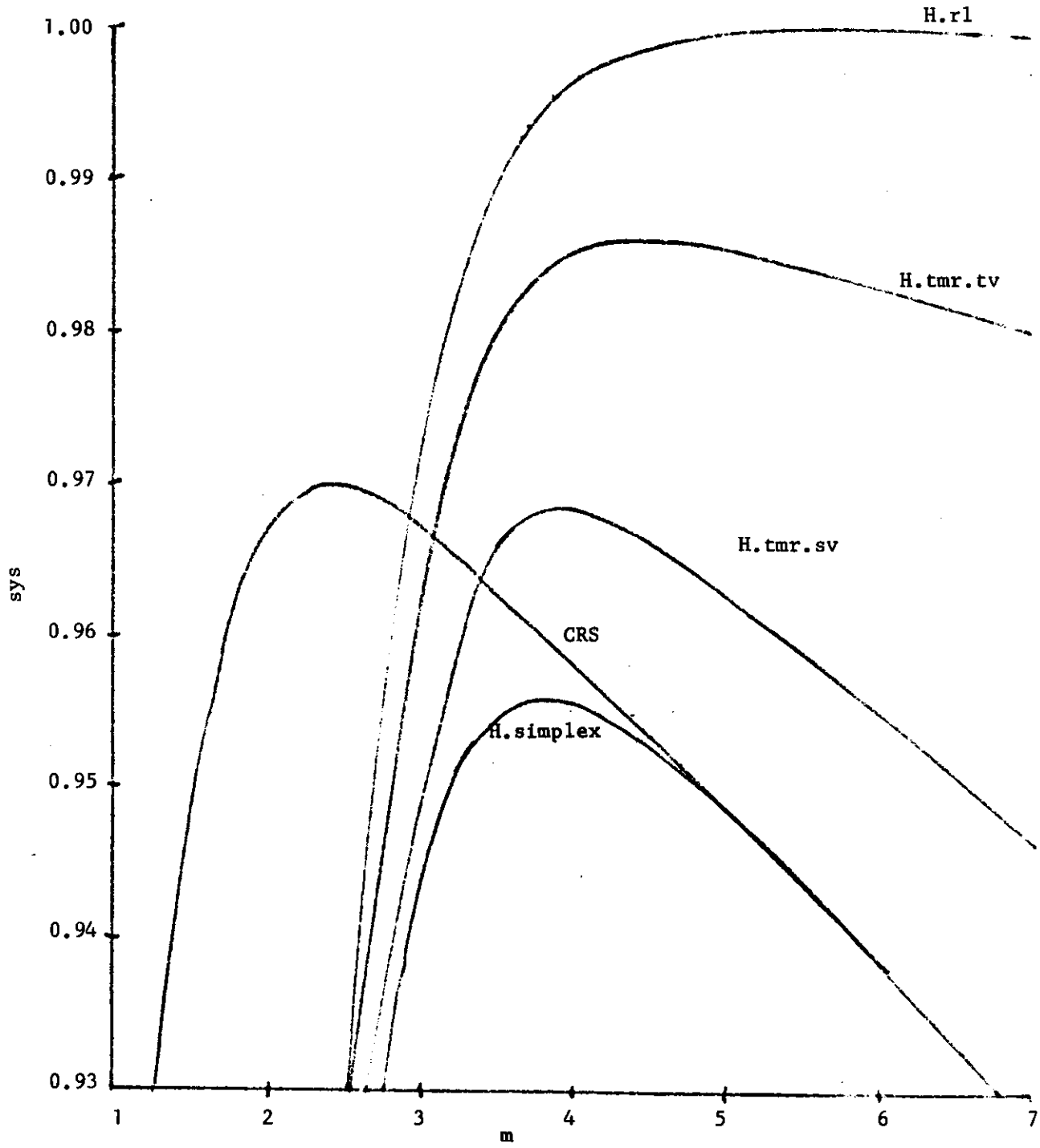


Figure 24. R_{sys} for various schemes as a function of m (for R=0.9, α=0.1).

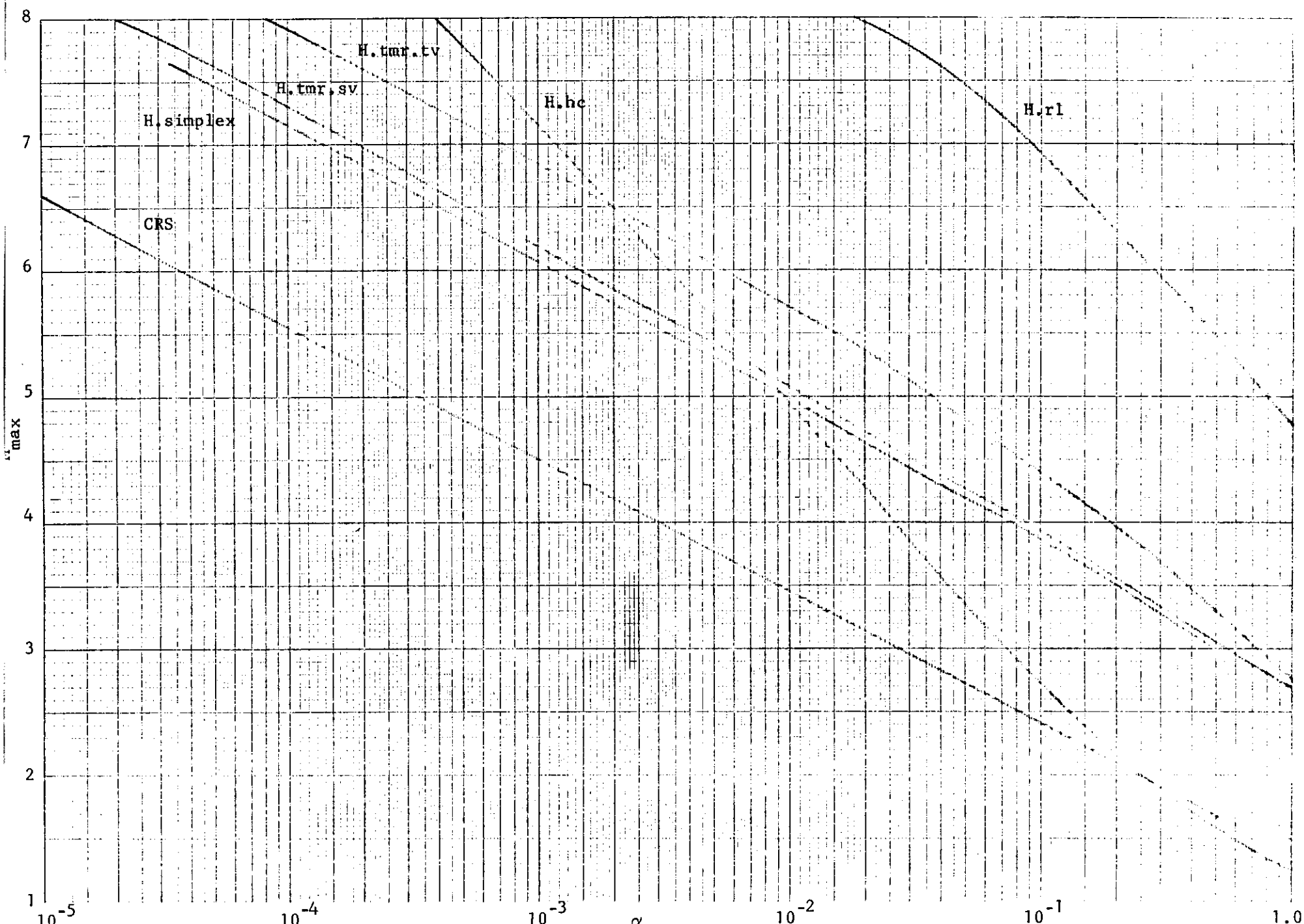


Figure 25. M_{max} as a function of α for various schemes (R=0.9).

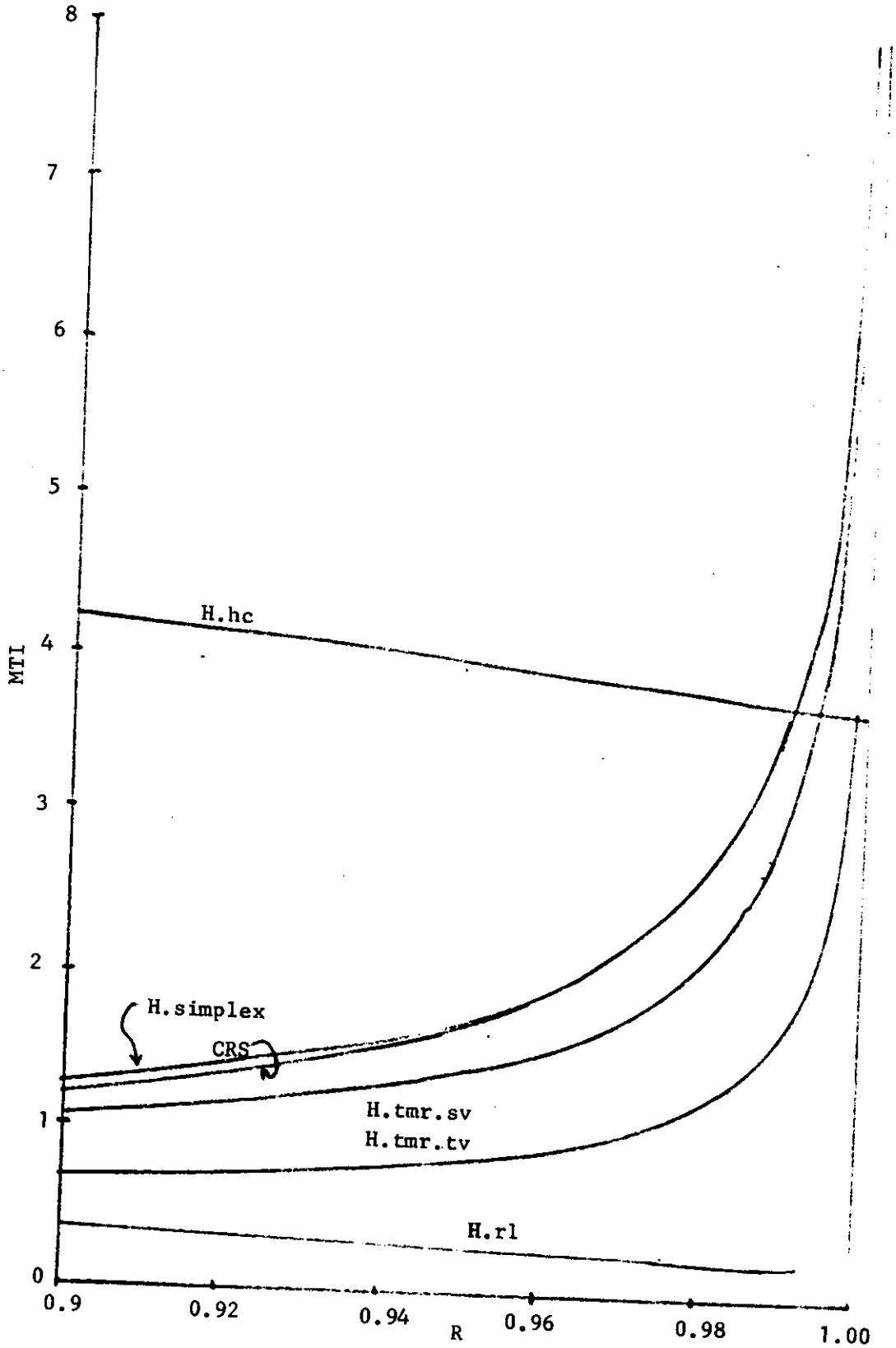


Figure 26. MTI of TMR over various schemes (m=4).