A Unifying Notation and Analysis of Modular Register Transfer (RT) Control

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Several register transfer (RT) module systems have been designed to provide the user with a set of design primitives (control modules and data modules) at a level higher than simple logic gates ($\wedge$, $\vee$, $\oplus$, etc.). The description of the control portion of these module sets is also intended to be at a level higher than boolean equations or logical diagrams. Several graphical representations have been proposed for the description of RT control networks composed of control modules but none is widely accepted. An acceptable representation should not only be descriptive but also analytical of the control flow. Two control flow problems are the detection of deadlocks and checking if a control network is safe. A deadlock is the situation in which some control modules are initiated to wait for certain signals which never occur, thus causing the operation of the complete network to stop. A control network is safe if each of its control modules does not receive a new control signal until it has completed its control action associated with a previous activation. Several representations such as the Petri Nets and the Graph Model of Computation (GMC) reported in the literature are capable of analyzing only certain proper subclasses of the systems they are capable of representing.

This thesis evaluates a number of existing representations for the control of modular, register transfer systems, unifies them by one notation and develops decision procedures, based on this notation, for the detection of deadlocks and checking for safeness of RT control networks. The decision procedures can be applied to all systems expressible by the notation which subsumes the Petri Net and the GMC.

To evaluate the existing representations, a taxonomy of representations is developed. The taxonomy classifies the representations by a number of dimensions, thus defining a space of representations. Each existing representation is a point in this space with its coordinates given by the parametric values the representation has for each dimension. Based on the taxonomy, several representations which include the Petri Net and the GMC are chosen as appropriate candidates. These representations are unified by a single notation, the Vector Addition System (VAS).

Two alternative control flow concepts: Liveness and Safeness (LS) and Proper Termination (PT) are abstractions for safeness and absence of deadlocks in control networks. Decision procedures for these concepts are developed on the vector addition system.

Applications of the decision procedures are demonstrated on existing module sets to detect deadlocks at the user level (erroneous interconnection of control modules) and at the module-set designer level (erroneous designs or limitations of the control modules). High level descriptions, expressed as VAS's, for the most commonly used control modules are provided. They model only the control flow in and out of a control module. Deadlocks at the user level can be detected by applying the decision procedures on the high level descriptions. For deadlocks at the designer level, behavioral descriptions, expressible in VAS's, that express the internal states and signal communication of the control modules are required. Previously unreported deadlocks at the designer level of two RT module sets are revealed by applying the decision procedures on their behavioral descriptions.

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