FABRICS II: A STATISTICAL SIMULATOR OF THE IC FABRICA PROCESS

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A STATISTICAL SIMULATOR OF THE IC FABRICATION PROCESS*

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Abstract

This paper describes a *Statistical Process Simulator* FABRICS 11 developed at Carnegie-Mellon University, as pan of a design verification/ optimization package. In this package the process simulaior is used with a multilevel circuit simulator, SAMSON pi to simulate KTs at the process, circuit and lope levels. Possible applications of FABRICS include verification and optimization of nominal process and circuit design, yield failure analysis. Hie current implementation of FABRICS II is briefly described and an example iflustnting the application of FABRICS II to process optimization is presented.

Introduction

Most ofthe VLSI design systems which are being developed at present employ a *structured (hierarchical) design methodology* PJ. A VLSI system is partitioned into modules with well defined nttriaccs. The symhews proceeds in a *top-down* manner from the high level *behavioral* description to the IC mask level Due to the complexity of VLSI e m u * the design cycle must contain a design verification feedback loop. Verification consists of checking whether the implementation meets the yccifications at various levels such as functional logic or layout levels, tea fully automated design systems (eg. silicon compiler) several verification tools (eg. drout extraction, logic SHWulation, dffign rule checking) may be imnrrntary because the system produces correct designs. However, there exists a need for IC performance evaluation prior to IC manufacturing. Computer simutarinn is the most powerful and widely used technique lor performance verification. For example a circuit simulaior. €4. SPICE is uaed to verify a aomtnof design. The accuracy of such a performance evaluation strongly depends on the accuracy of the device model parameters used in the 1imulation.

Generally, the *#mk* set of model parameters present in circuit simulators is not valid for a particular fabrication process, so these parameters have to be extracted from measurements made on awMiiactured devices. The extraction of model parameter/is difficult because they are not independent Hence, it may be that the extracted values are significantly different from the real<>nes.

An alternative method ft* determining device parameters is to use a *Process Simulator* which contains physical models of fabrication sups and device modcK. Such a amiibior may be tuned to a particular process by means ofa few typical in-process measurements, and would then generate full sets of model parameters which are in good agreement with data extracted from measurements.

Due to unavoidable fluctuations which are inherent in the IC fabrication process, device parameters, and consequently IC performances, are subject to variations. Ideally an IC should be designed in such a way that variations in its performances, due to the fluctuations which occur in a normal manufacturing process, are within allowable tolerances. Traditionally. IC designers performed *worst ease omatyus* by varying device parameters. However, since this approach did not take into account the dependencies among these parameters, die resulting designs were often too conservative. Moreover, adjustments in design rules which were often made raiiifrl fncrcase si the chip area* which could result in the decrease in the yield value because of the catastrophic defects.

Recently* an axreased amount of effort has been directed •jwaras stausucaf oesign memoes, LC. metnoos n wmen me objective is to maximize manufacturing yield. Yield maximization is performed in terms of process and IC layout parameters [31 Accurate yield prediction is of crucial importance in these methods, and it is usually done by multiple evaluation of circuil performance, each evaluation being carried out with a different set of device model parameters, hi order to obtain accurate results, the joint probability density function *(jpdfl* which describes the distribution of device model parameters must be dose to that found in reality. This is especially important for monolithic KTs where the correlation coefficients between device parameters arc important and agreement in means and variances is not saflldem. Data samples suitable for use in a circuit simulator, and with the correctjpdf. can be generated by a *StatisticalProcessSimulator*

In this paper we present a statistical process simtulaior, FABRICS II. Since the methodology behind statistical process simulation was presented in J4J. here we focus our attention on the description of the structure of FABRICS II. the models which are impkmemed in the current vcrskwuand the incorporation of FABRICS II iwo a design verification1/optMzation package for KTs,

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ModcK far Slatktkal Simulation

Traditional approaches to process simulation (eg. programs ike SUPREM |5J> employ *numerical moMs* of the fabrication steps. These modcK which arc described by puntal differential equations <c.g.diffu<dun equation!, are solved using numerical techniques lo produce the nominal profiles of impurities in siiicun. The impurity profiles are then input to device simulator* (e.g.SEDAN J6J). in which semiconductor device models are described by a system of partial differential equations (e.g. Foissonoranspon and continuity equations). These equations aft solved numerically to produce device parameters. While the accuracy of simulation results obuined from these simulators is high, these approaches become prohibitively expensive for statistical investigations, due to the complexity of the models used Furthermore, identification of some input parameter is difficult and these programs lack a direct interface to dram simulators.

To alleviate these difficulties, we proposed [7] the toe of analytical models which art solutions of the partial (fiflereotiaJ equations that describe each fabrication step, under a set of restricted or simplifying conditions, which have been found to yield reasonable results. The input to such a model would consist *of process parameters,* such as times and temperatures of diffusions, or doses »d energies of ions in implantation, output parameters of previous modeling steps, and *process disturbances.* These disturbances are modeled as physical parameters, such as diffushrities of impurity atoms and misalignment between two photolithographic masks, which art *mndom variables* with probability distributions determined by *tuning* to a particular fcbrication process. In a similar fashion, the device models are also analytic using the output of the fabrication step models, and device layout to calculate the device parameters. For a more complete description of these models, and of the tuning procedure, see W-

It should be noted that recenUy analytical modeling techniques have become more popular in the area of proces and device simulation. Several programs have been developed in which either analytical models or a combination of numerical and analytical models arc implemented^ two-dimensional process sumilator.SUPRA |8) or process and device simulator, PRIDE [9]). These approaches offer a reasonable compromise between the accuracy and efficiency of smiulaiion.

Structure of the Simulator

FABRICS II is the second version of the simulator described in |4]. This version is written in PASCAL and currently row on a VAX 11/780 computer under the UNIX and VMS operating systems. New models of both fabrication steps and semiconductor devices have been added which c!k>* for simulation of a variety of different pmtts&cs including NMOS.CMOS and bipolar. 1 he structure of the simulator lus been significantly changed to make it modular. It is now very easy to add a new model or modify an existing one without altering the remaining pan of the simulator. FABRICS II is composed of two major parts, called FABI and FABI each of which contains a collection of analytic models as described above.

Process Simulator. FABI. contains models of manufacturing operations. The structure of FABI is shown in Fig.1. The input consists of process parameters, process disturbances, and run control parameters. The following models of the fabrication sups are included:

1. Diffusion of impurities into silicon. Diffusion is modeled as a two-step process consisting of predeposkion and drive-in. Segregation of impurity atoms between silicon and silicon dioxide is taken into account Diffusion models for three basic dopants, ie. phosphorus, boron and arsenic are included.

2. Ion Implantation. Ion implanted profiles are determined from an analytical model. Models for annealing and thermal redistribution of ion-implanted impurity atoms art also included

3. Thermal oxidation. The model for oxide growth implemented in FABI takes into account the changes in the oxidation rate due to various oxidizing ambients (steam, dry or wet oxygen), heavily doped substrates and partial pressure of oxygen.

4. Photolithography. Statistical model for lithography operations is implemented which accounts for linewidth inaccuracy caused by misalignment, and by fluctuations inherent in optical and etching operations.

i. Surface treatment processes and 1X20103 deposition are modeled statistically by the random variables representing process fluctuations (cLgJurfece potential surface recombination velocity, surface state density, specific contact resistance).

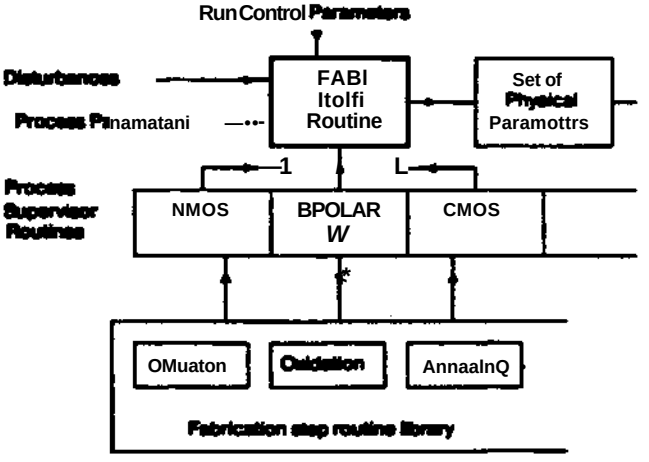


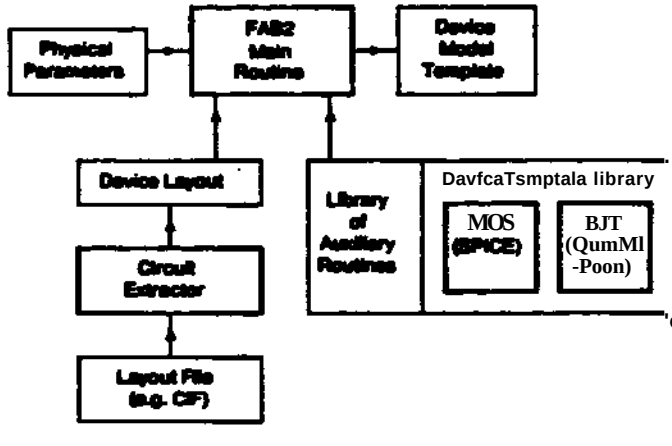
Fig.1. 9tructvf» of FAB1

FAB] abo contains models for in-line measurements such as riicct resistances and junction depths of diffusion layers, and threshold volumes of MOS transistor. A detailed description of the mudeb implemented in a current version of the simulator can be found in |1Q| Subroutines whicli employ the models of the fabrication steps together with the corresponding in~tine measurement models are stored in a ttwary. Each of the fabrication processes which can be simulated by FAB1 hat a p v c w j » A m w r o u t i n e w h k h c o n t a m a l i t t t f ^ broutine calls for manufacturing flcp routines sored in a library. This process supervisor, which is similar to the fabrication process flow chart process simulator for a particular manufacturing process may be created The main routine of FAB1 panes the input data and outputs the physical parameters generated in the simulator, such as parameters of impurity profiles or oiide thicknesses, to the physical ftarnirmm fiataÎlair.

Device Simittaflf, FAB2. uses the physical parameters generated in FABL combined with the layout dimensions of semiconductor devices, to produce the device model parameters, such as the parameters of the Shichman-Hodges model of *m* MOS transistor or the Gummd-Poon node) of a bipolar transistor. These parameters can be used in a circuit snmlator to predict the performance ofthe circuit,

In me current trnpiementaüott, mere cm a Horary or me device models. The main routine of FAB2 panes a model template and determines a list of parameters which have to be calculMcd. Then the model parameters are computed using functions ftored in a device model library, and ned to *fiU* a model *ttmpitat* to be used in the cirttrt WHufator. OHrest version of the device model Mbrary cosfans models of semiconductor devices ÏHHpIcflBSHted ÏHI SPICE and SAMSON 111.

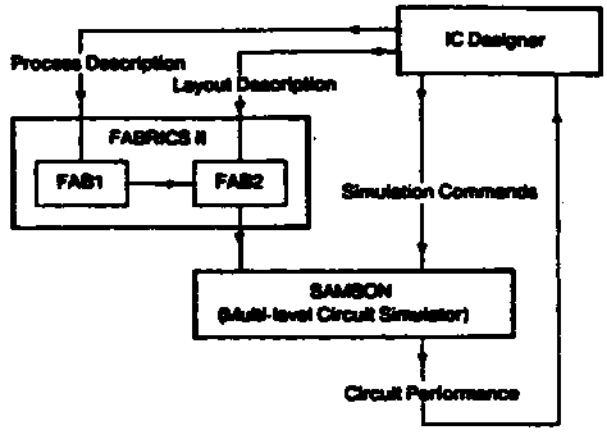
Fig. 2 shows the sructure of FAB2. Note thai information •bout the dimensions of the various devices is derived from a layout description of the chip (tg. a OF fite) using a circuit extractor (11} This layout information is dfoded into two pans: device dimensions, which are used in FAB2 to calculate device FABRICS II to produce R-C type dements, *md* used in a circuit simulator to determine delays between circuit blocks.



Rg.2. Structure of PAB2

Applications and Examples

A design verification/optimization package consist of FABRICS II and SAMSON. The anictiire of ths package is Aown in RgJ. This package may be used « a design tool that is capable of amuUtng a given circuit/layout at the process, circuit and logic levels. The linking of thcac prr^rams relieves the designer of the *usk* cif transbtini*, the output of one program into proper input for another program.



Ra.3. Structure ot Skmitatkm System withPAMUCSH

FABRICS IK in the statistical mode, may be used to generate data samples that can be used for yield prediction, statistical verification aid yield maximization. Current work is being done on fault diagnosis of an IC manufacturing process using FABRICS II [121 Such a simulator can also be used for process control and as a basis for a quality control system for an IC fabrication process.

To ilkistratc how FABRICS II can be *>plied to process optimization, we considered an example of a 64 bit x 64 bit dynamic RAM cefliinplememedmN MOS technology [13]. The circuit oonsisis of one 3-transistor memory cell, row decoder and driver, column decoder aid driver, read-write dock driven, and prechaige circuit The entire circuit contains 74 MOS tnnsisurs. We investigated the effect of changes of process parameters on ctauit performance. In particular, the influence of gate oxidation time on power chssipaLioo and read cyde access time w « investigated. An experiment was performed in which gate oxidation time was varied, and for each value of time a ample of device paraaeten was gnemed by FABRICS H. The simulator was tuned to a ftVKtvd NMOS fabrication process. The resultant device parameters generated by FABRICS II were automatically input to SPICE for chcuit mutation. The results obtained from these ciperimeim are riwwn in Rg.4 and Fig3. As indicated in Rg.4. power (tetpation monotonically decreases wHii me •Kiian. HI me gate onsanon ujne. ims s cameo oy the fret thai the increased oxide thkknes rtwhs in a decreased intrinsic transconductance of the MOS transistor, which <causes smaller drain currents aKL conseQuentJy, smaller power dnsipation. FigJ indicaies that the acces time monotonically

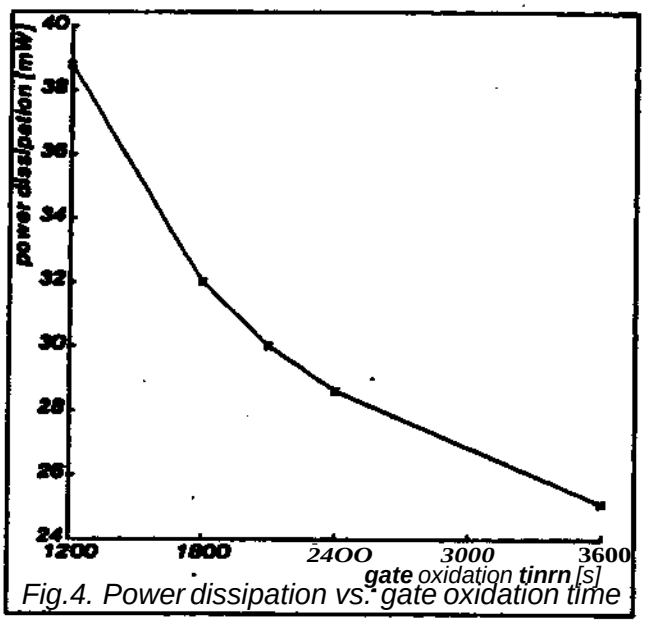


Fig.4. Power dissipation vs. gate oxidation time

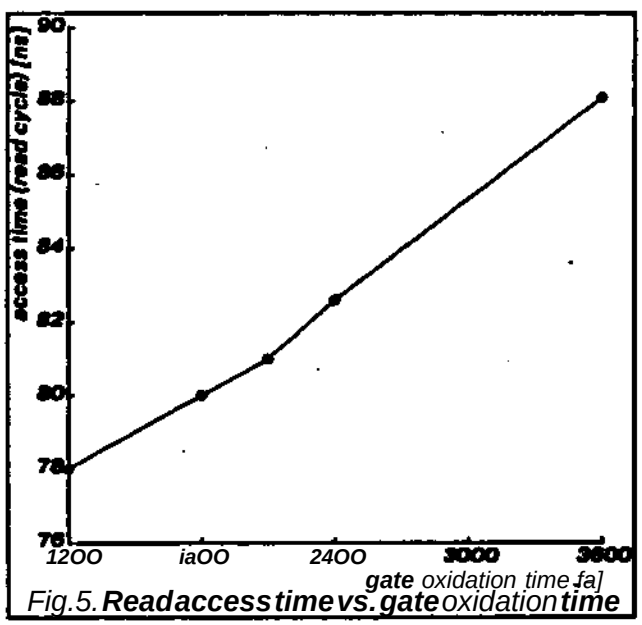


Fig.5. Read access time vs. gate oxidation time

increases with the increase in gate oxidation time. Tliisiscaused by the fàct that the decreased intrinsic tfansoonductanoe of the MOS transistor causes a drop in speed. Hence, it is possible to investigate the power-speed trade-off for various KT designs.

FABRICS II has been tuned to a standard CMOS fabrication process and the accuracy of simulation proved to be good when compared to the measurement results and SUPREM simulation/This comparison will be demonstrated in the conference presentation.

References

I. K. A. Sakalbh and S. W. Director. MAn Event Driven Approach for Mixed Gate and Circuit Level Simulation," *Proceedings of ISC AS.* IEEE. Rome. May 1982.

1 S.W. Director. AC Parker. D.P. Siewiorek and D.E ThomasJr.. **A Design Methodology and Computer Aids for Digital VLSI Systems." *IEEE Trans, on Circuits and Systems.* VoL CAS-28. No. 7. July 1981. pp. 634-645.

3. W. Maly. AJ. Strojwas and S.W. Director. "Fabrication Based Statistical Design of Monolithic ICs." *Proceedings of ISC AS.* Chicago. April 1981. pp. 135-138.

4. W.Maly and A. J.Strojwas. "Statistical Simulation of the IC Manufacturing Process." *IEEE Trans. CAD.* VoL L No. 3.1982..

5. D.A. Antoniacfis. S.E Hansen and R.W. Dutton. "SUPREM 11 - A Program for IC Process Modeling and Simulation." Tech. report 5019-2, Stanford Electronics Laboratories. June 1978.

6. D.C. D'Avanzo. M.Vanzi and R.W. Dutton. "One-Dimensiona] Semiconductor Device Analysis (SEDANX" Tech. report G-201-5, Stanford Electronics Laboratories, October 1979.

7. W.Maly and A.J. Strojwas. "Simulation of bipolar dements for statistical circuit design." *Proceeding? of ISC AS.* July 1979. pp. 788-79L

8. Technology Modeling Associates. *SUPRA - Two Dimensional Process Analysis Program.* 1A-led,1981.

9. J.R. Pfiester. Integrated Grains Uboratory^tanford University. *PRIDE • Portable Process and Device Design.* 1961.

10. S.R. Nassif. A.J. Strojwas and S.W. Director. Department of Electrical Engineering. Carnegie-Mellon University. *FABRICS II • A Statistical Simulator of the IC Fabrication Process.* 1981

II. A. Gupta. "ACE: A Circuit Extractor." VLSI Document V105.CSD.Carnegic-Mdlon University.

12. A. J. Strojwas, *A Pattern Recognition Based System for IC Failure Analysis.* PhD dissertation. Carnegie-Mellon University. September 1982.

13. H. Walker, private communication^