FABRICATION BASED STATISTICAL DESIGN OF MONOLITHIC IC'S

W. Maly, A.J. Strojwas, and S.W.Director

DRC-18-32-81

September 1981

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W.Maiy[2],A.J.Strojwas and S.W.Director

Department of Sectricai Engineering,
Camegie-MeHon Unfversrty
Rttsburgh,PA 15213

Abstract

In this paper we discuss the statement of Yield Maximization problem and the choice of design parameters when considering statistical design of monolithic ICs. Specifically, yield maximization cannot be carried out in terms of the nominal values of the eiecxncai parameiers oc iw s eminents. MI extension to me exisdng methods and a new formulation of the Yield Maximization problem for monolithic ICs is proposed. The necessity of employing a SNiHjlator of the manufacturing process • whIch retafess a clrcuit eiecxncat oenavtor to tne pnyscaiiy oseignanie parameters , is shown.

1. Introduction

A number of statistical design aids for yield estimation and optimization and worst case analysis have been developed (1.2.3. 4) to help the circuit designer wherever the random fluctuations inherent in the manufacturing process have to be considered. Specifically, for the case of the statistical design of monolithic ICs, me YleW MaxtmizatK^ (YM) is the cemrml issue. Usuafty the yield maximization problem was formalized in the following manner.

Let the circuit to be designed be described by a set of algebraic and differential equations:

$$g_k(\dot{y},y,t,a,X) = 0 \quad \text{for } k = 1,2,\ldots,n_g \qquad (1)$$

where

- y- is a vector of voltages and currents
- t- Is time
- a- is a vector of the circuit parameters which can be assumed to be constant
- X- is a vector of random variables[3] representing circuit parameters which are randomly varying due to imperfections and distrubances in the manufacturing process, (typically resistances and capacitances, threshold voltage of MOS transistors etc.)

Let the constraints of the circuit performance be described by a set of inequalities:

$$*_k(x) \equiv \int_0^{t_f} e p_k(y,y,t,a,c)dt \leq 0 \quad \text{for } k = 1,2,\ldots,n_c \qquad (2)$$

where x is a particular value of X. Thus the set

$$1^{\wedge} \equiv \{x : *_k(x) \leq 0 \text{ for } k = 1,A,\wedge,n_c\} \qquad (3)$$

which is called the acegotability or feasible reoion, represents the set of realizations of the random variable X (i.e~ all particular values of circuit parameters) for which the circuit meets the desired requirements. Assuming that X is described by a joint probability density function[4] (jpdf). $f_X(x,p_X^1,p_X^2,\ldots)$ a vector of mean values of X and p_X^2 is a vector of higher order moments of X, the yield, Y can be denned as:

$$Y = \int_{R_X} f(x,p_X^1,p_X^2)\,dx \qquad (4)$$

In order to state the yield maximization problem and solve it by the existing methods, it is necessary to make the following two assumptions:

A1: It is possible to obtain any desired value of p^ by means of adjusting the process parameters and/or the layout of the IC

A2: The vector of higher order moments, p| is independent of the circuit and the process parameters.

Under these assumptions, the yield maximization problem should be stated as the following optimization problem:

$$\max_{p_X^1} \int_{R_X} f(x,p_X^1,p_X^2)\,dx = Y \qquad (5)$$

Unfortunately, assumptions A1 and A2 are not necessarily valid for monolithic IC applications. In particular

0 Some components of p^, which are the optimization variables, are not designable in the sense that they are not necessarily adjustable to any given solution of (5). For example, the mean value of the threshold voltage of an MCS transistor cannot be arbitrarily adjusted to any desired value but can only be determined for a particular process and then only slightly modified.

it) In general, the components of pj are not independent of one another. Therefore, it is not always physically possible to obtain a specified combination of values amongst the components of p^. For example, the mean values of & of two n-p-n integrated transistors are strongly related to one another.

iit) The higher order moments, denoted by p^ are not independent of p^{λ} For example, the mean and variance of the resistance of a monolithic resistor are dependent on its geometry.

In this paper we show that by judicious choice of truly independent designable parameters and an alternate formulation of the yield maximization problem we can develop a method which

[1] This research was funded in part by the National Science Foundatkn under Grant ECS79-23191

[2] *On* leave from Technical Unwersrty of Warsaw. Poland

[3] An random variables are denoted by capital letters.

[4] For normally distributed random variables X me jpdf is fully characterized by ma- first and second order moments, i.e. by vector of mean values $m_i^{\wedge}$ and covariance matrix $\pounds_{\wedge}$

is more suitable for the design of monolithic iC's than those previously reported. Furthermore, we show that a key step in the yield maximization problem is the simulation of the manufacturing process. In particular we introduce the use of a process simulator (5) into the design procedure.

2. Independently Desicmable Parameters in Yield Maximization of Monolithic IC's

We wish to determine under what conditions the solution of (5), is technologically reatfrable. Assume that the manufacturing process can be characterized by a vector of deterministic , physically independent and controllable quantities (e.g. temperatures, diffusion times, mask dimensions. etc.),denoted by z and called primary design variables. Further let 0 denote the set of uncontrollable disturbances, inherent in the manufacturing process. Hence the parameters of the jpdf of X are dependent upon both z and 0. Observe that while the values of p£ can be controlled by changing z . the set of technotogicaiiy realfrahki combinations is restricted due, in part .to the existence of 0. Thus there may exist the solutions of (5) which cannot be obtained by means of changes of *z* only. Specifically, the solution of (5) . p^{0*} , is technologically realizable only if there exists a z^{0*} such that

it wifl always be possible to find a i^{00*} which satisfies (6) if the components of the vector p£ » {p£$_r$ p^, -} are independent and strictly monotontc functions of components of the vector z . We call the random variable X_i, which is a component of X, whose mean, p^ is a strictly monothonic function of a primary design variable z. a deskmable random variable. Furthermore, if we can change the value of $p^{\wedge}_{l}$ while keeping the other components of p£ constant then X_l is said to be an independently dasionable random variable. Hence, a solution of (5) will be technologically realizable if every component of X is an independently designable random variable.

We now wish to illustrate the above general considerations and determine which parameters are the primary design variables and which parameters are the independently designable random variables for the case of monolithic integrated circuits. In order to motivate this discussion consider me following simple example. Let w and I be the width and length of a rectangular window in a photolithographic mask used to fabricate an integrated resistor. They constitute the primary design variables in this example. Due to imperfections in the photolithographic process the dimensions of this window in SiO_2 are described by random variables L and W, respectively. Assume for simplicity that W » w + IF and L « I • AF, where AF is a zero mean normally distributed random variable with standard deviation *a*^ which represents the disturbance in the photolithographic process. One can show that if both I and w are much greater than 3 * ^ then F«L/W is a normally distributed random variable with mean ny » l/w and variance

$$\sigma_F^2 = \quad ^2\sigma_{\Delta F}^2 \tag{7}$$

Furthermore, it can be shown that the actual resistance of the integrated resistor is also a normally distributed random variable R suchthatR * F*Rs with mean m^ and variance <t£ given by

$$m_R = \frac{1}{w} m_{Rs} \tag{8}$$

$$\sigma_R^2 = m_{Rs}^2[(w-l)/w^2]^2\sigma_{\Delta F}^2 + \left(\frac{1}{w}\right)^2\sigma_{Rs}^2 \tag{9}$$

where Rs is a normally distributed random variable with mean m ^ and standard deviation σ_{Rs} which represents the sheet resistance. Thus R is a d^Hanabte random variable because any specific mean of its resistance can be obtained by adjusting the ratio l/w. Moreover, it is an independently desionable random variable because the mean values of the resistance of the different resistors in the circuit can be chosen independently of one another. Hence, it would appear that the nominal resistance values of integrated resistors could be used as optimization variables .p^ for solving the YM problem (5). However, since m^ and $<x_R$ are dependent on each other this choice of variables would violate assumption A2.

Note that this observation can be extended to all electrical parameters of monolithic elements because both the nominal values and higher order moments of these electrical parameters are related to the mean and variances of the mask dimensions, as weM as their ratios or window areas. (The moments of dimension ratios or areas are dependent of each other (e.g. see (7)). Hence none of the moments of electrical parameters of monolithic elements can be used as the optimization variable in the YM problem (5).

Note that for the examples discussed above, we can choose as optimization variables, instead of p^, the means of L and W. (L and W are independently designable random* variables because m_L » I and m^ » w and their variances are independent of m^ and nry, respectively). In general, since any IC design can be described *In* terms of the mask dimensions, then the mean of the random variable Z. » r + AF, pi , representing the dimensions of the IC elements, which are related to the mask dimensions z and disturbances in the photolithographic process AF, can be chosen tobetr»optin«zatk>nvanablerntrmYMpro61eni(5).

3. Yield Maximization Using the Process Simulation Technique

Since the components of X cannot represent the electrical parameters of the IC the yield maximization problem (5), for case of monotiihic ICs, has to be modified. Towards this end we replace the circuit equations (1) by:

$$g_k(y,y.t^*x)\text{-»}Q. \quad k = 1,2,\ldots,n_d \tag{10}$$

$$c_j(x,Z) = 0, \quad j = 1,2,\ldots,n_p \tag{11}$$

where expression (11) models the manufacturing process. Using (10) , (11) and (2) one can define the feasible region $\&_z$ in the space defined by 2. We can now formally state the yield maximization problem as

$$\int_{R_Z} p_Z^1 p_z^2 dz \tag{12}$$

where Uz. p*, pS. pi-and pfare the ipdf. means and higher order moments of *t* respectively. Thus by adding constraints describing the manufacturing process to the previous statement of the YM problem, and properly choosing elements of Z. the YM problem of monolithic ICs can be solved by the methods proposed previously d).

Observe that in general, the dimension of Z is much larger than the dimension of X.(For instance, the number of variables describing the layout coordinates of the zigzag resistor is much larger than the number of its electrical parameters). Thus, the computational expense of approximation to the feasible region R_r in the space of independently designable parameters Z could be much larger than the computational expense of approximating R_x in the space of circuit electrical parameters X. Thus we we propose the following approach.

Assume that we have an •approximation, H_x, to the feasible region R_x. Since the random variable X is dependent on Z. wntch is an independently designable random variable related to the primary design variable *z*. then at feast some moments of X are also dependent on *z*. Let p̃^ and p̃£ denote those moments of X which are dependent on *z*. and let 0_x^1 and $\tilde{p}_x^*$ denote those moments which are independent of *z*. Hence pi»{P̃x • ffj) **<* P̃x^{a}^^{2}x • $$* The YM orcblem can now be stated in the following way:

$$\max_{z} \int_{H_X} f_X\left[x, \bar{p}_X^1, \sigma_X^1, \bar{p}_X^2, \sigma_X^2\right] dx \qquad (13)$$

Note that any solution of (13) is technologically realizable and because we are in a lower dimensional space, the cost of the solution of (13) should be less than cost of the solution of (12). Of course, a key step in being able to solve (13) is the simulation of $\bar{p}_X^1$ and $\bar{p}_X^2$.

We now consider the process simulation technique we need for generating $\bar{p}_X^1$ and $\bar{p}_X^2$. As we stated earlier

$$X = P(z,D) \qquad (14)$$

where P ( ) is a model of the manufacturing process relating the elctrical circuit parameters X to z and D. The disturbance, D, is most easily simulated using an appropriate random number generator. The advantage of such an approach is that the disturbances of the process are characteristic of a given technology and manufacturing facility, but are independent of the particular circuit to be designed. Hence, the jpdf describing D, $f_D(d)$, needs to be identified only once for each process. Hence, employing (14) we can estimate moments of X in terms of z and therefore solve (13). In the next sections we describe the process simulator which has the capabilities we need.

4. Examples

In our investigation the statistical process simulator FABRICS (FABRication Process of Bipolar Integrated Circuits Simulator) was employed for simulating (14). A detailed description of this simulator is beyond the scope of this paper (see (5, 6, 7)). Suffice it to say that FABRICS was used to generate the data samples composed of electrical parameters of typical bipolar IC elements (i.e., samples of random variable X).

In this section we examine three examples which serve to illustrate the following observations. The first example illustrates the dependence of p_X^1 and p_X^2 on one another. The second example exhibits the fact that even if the nominal values, p_X^1, are constant, the higher moments, p_X^2, can be modified by means of layout changes . The third example demonstrates the computational efficiency of the proposed process simulation technique for solving the YM problem (13).

In each of the examples we have assumed that all of the process parameters are constant and the design variables are mask dimensions. Note that the results reported below were obtained using FABRICS tuned to a real manufacturing process, thus the data presented is physically meaningful.

Example 1.

Consider the following elements of a bipolar integrated circuit: three base diffusion resistors, R_1, R_2, R_3, and one n-p-n transistor. We assumed a fixed layout for the two resistors R_1 and R_2 and for the n-p-n transistor. The length of resistor R_3 was also assumed to be constant while its width, w_3, was treated as a primary design variable,z. The question was whether the changes of w_3 would affect all of the parameters of the jpdf describing the random variables R_1, R_2, R_3 and β of the transistor. Using FABRICS we generated 900 samples (each sample was composed of values for R_1, R_2, R_3 and β) for three values of w_3. The projections of four dimensional scatterplots onto the planes (R_1 x R_3), (R_2xR_3) and (β x R_3) are shown in Fig. 1. We can conclude that the changes of w_3 not only affect m_{R3} and σ_{R3} (according to formulas (7),(8) and (9)) but also the correlation factors of R_3 with the other resistors and β).

Example 2.

We now consider an IC which contains among other two resistors, R_1 and R_2 and an n-p-n bipolar transistor. The primary design variable,z, in this example is the layout scaling factor,λ , which is a quantity by which all element dimensions are multiplied. In Fig. 2 the scatterplots of R_1 and R_2, and R_1 and β, for λ = 1.0 are shown. Similar plots for λ = .5 are shown in Fig. 3. Comparing these two figures we observe that the means of R_1, R_2 and β remain almost unchanged while standard deviations increase and correlation factors decrease if λ decreases. Thus, we see that yield can be affected by holding the nominal values of the designable parameters constant and change the higher order moments which depend upon the scaling factor λ.

Example 3.

We wish to determine the dependence of the yield of the Motorola MC1530 operational amplifier (8) on the layout scaling factor λ. Towards this end we define acceptable performance in terms of the following inequalities:

$$-2mV \le V_{in\ off} \le 2mV, \quad I_{BIAS} \le 6\mu A, \quad A_d \ge 8{,}000$$

where $V_{in\ off}$ is the dc input offset voltage, I_{BIAS} is the input bias current, and A_d is the differential mode gain.

The yield estimators for several values of λ (λ = .2, .3, .5, .8, 1.0, 1.5, and 2.0) were found by means of the Monte Carlo method ,using FABRICS and BIAS-D (9), to evaluate $V_{in\ off}$, I_{BIAS} and A_d and then computing the yield. The relation obtained between yield and λ is shown in fig. 4. We found that the yield drop for λ<1 was due to an increase of σ_{A_d} which was caused by an increase of variances of element parameters. Observe that for increased values of λ, the yield never reaches 100%. This means that the Op Amp yield is determined not only by the designable part of X. Thus, as we have pointed out in the YM problem (13), the designable part of X should be distinguished from its undesignable part. We found also that the CPU time required for process simulation was less than 10% of the time required for circuit simulation.

5. Conclusions

In this paper we have discussed two formulations of the YM problem suitable for the design of monolithic IC's. We have defined the conditions under which the method proposed in (1) can be used for monolithic IC's. We have also proposed a different statement of the YM problem which seems to be suitable when large number of the IC's elements must be taken into account.

We have found that,in general, in order to solve the YM problem for monolithic IC's it is necessary:

i) to define the set of independently designable variables

ii)to use a process simulator to relate the layout of the circuit and process parameters to the circuit parameters.

We have also found that the optimization technique employed for solving the YM problem for the monolithic IC's has to take into account the fact that the space of randomly varying parameters determining circuit yield contains elements which cannot be designed and must be treated as a disturbance only.

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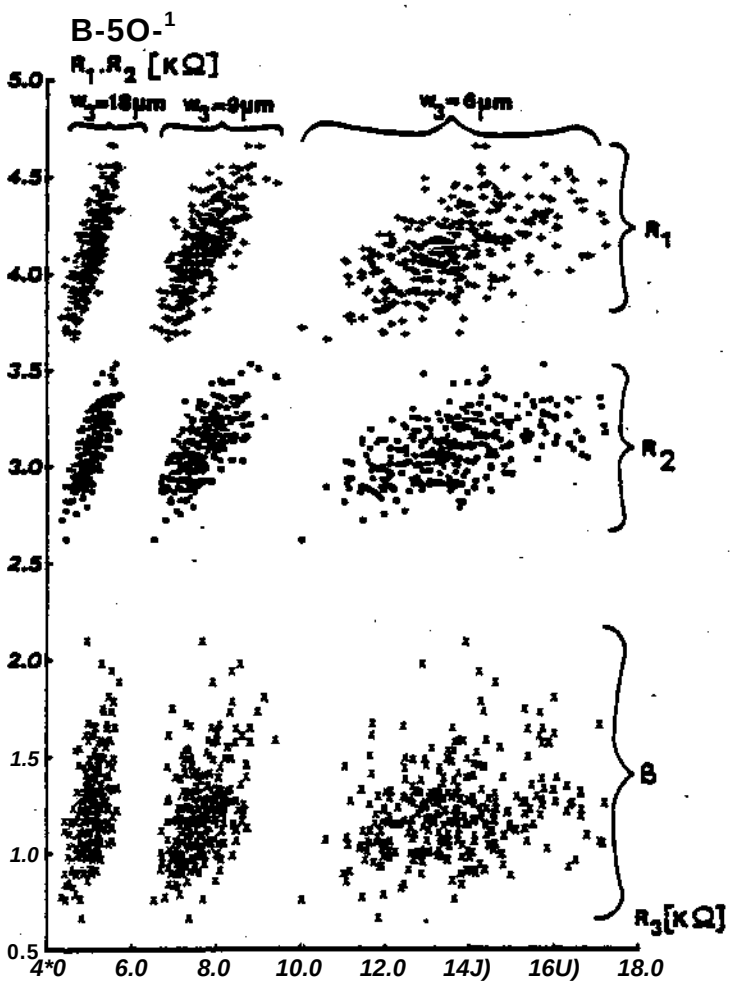
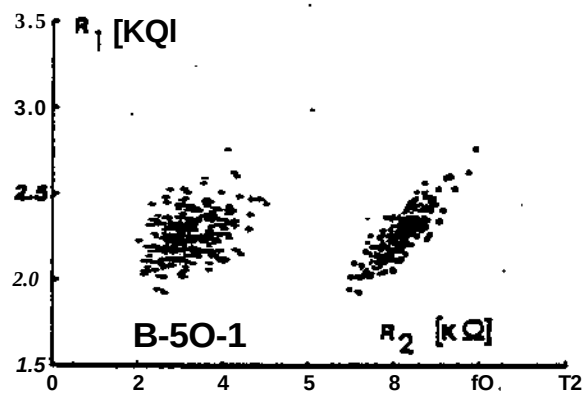
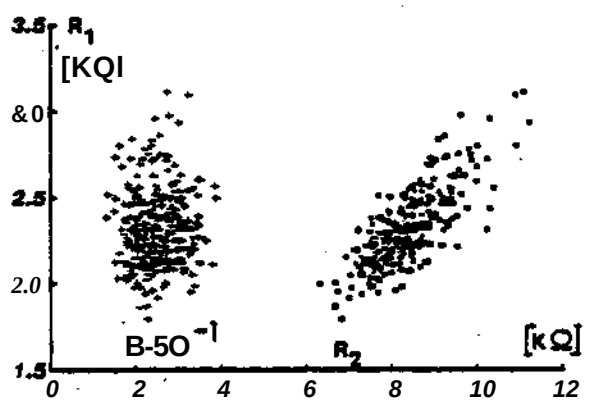


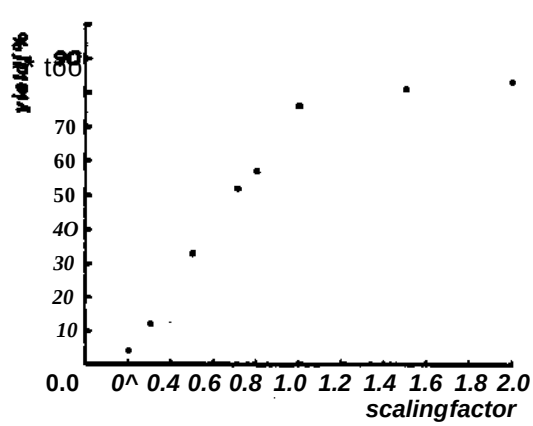
Fig.1. ***Scatterpiots of*** **ft,,** ***R2and*** **8** ***vs. l?3***



Hg.2. ***Scatterpiots of R^ vs.*** **S and fl^/or A a t.**



Flg.3. ***Scatterpiots of*** **ft,** ***vs.*** **B** ***and R2 for*** **As.5,**



Ftg.4. Yield vs. Layout Scaling Factor A.